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ITM-6292N

IEEE 802.11ah Wi-Fi Solution + MCU SoC

V0.1

Revision History

Date	Revision Content	Revised By	Version
2023/04/18	- Initial released	H.W.	0.1
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Contents

1. General Description

ITM-6292N is a highly integrated baseband (MAC & PHY), Sub 1 GHz radio transceiver and ADC/DAC single chip. It is fully compliant with the IEEE 802.11ah standard which is long-range and low-power version of Wi- Fi standard. Its 1/2/4 MHz channel bandwidth support yields 150 Kbps to 15 Mbps PHY rate that can sup- port low-rate sensor to high-rate surveillance camera applications. The self-contained Wi-Fi networking with huge range of data throughput offers the ideal solution to add Wi-Fi connectivity to IoT products.

Two embedded ARM processors, Cortex-M0 and Cortex-M3, in the ITM-6292N offers rich processing power to accommodate Wi-Fi subsystem as well as user application in a single Wi-Fi SoC. ITM-6292N also includes two host interfaces, HSPI and UART, and many peripherals such as general SPI, I2C, UART, PWM, auxiliary ADC and GPIOs. In addition, it provides a memory large enough for both AP (access point) and STA (station) op- eration. The low-leakage retention memory can be used to store code and data necessary for fast wake-up from deep-sleep mode.

Brickcom proprietary RF transceiver is a complete radio front-end optimized for Sub 1 GHz band. It has fully integrated pre-power amplifier, fractional-N synthesizer and the capability to support various com- mercial external FEM (front-end module) devices. The internal and digitally controlled gain stages at RF and baseband provide low noise figure and large dynamic range of the receiver. Furthermore, the transmitter has more than 30 dB gain range, which offers a wide range of output power.

The PMS (power management system) inside of the ITM-6292N contains a highly efficient buck converter, sev- eral LDO (low drop-out voltage) regulators, and a reference band-gap circuit.

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1.1 Features

The main features of ITM-6292N are represented as follows:

- CPU
  - ARM Cortex-M3 for Application at max. 48 MHz
  - ARM Cortex-M0 for IEEE 802.11ah WLAN
  - Clock Frequencies for both processors
    - 32/48 MHz
  - Mailbox for commuation between Cortex-M0 and Cortex-M3

- Internal Memory
  - 32KB Boot ROM_M3
  - 32KB Boot ROM_M0
  - 752KB System SRAM
    - SRAM0 : 256KB
    - SRAM1 : 256KB
    - SRAM2 : 224KB
    - SRAM_RET : 16KB
- MAC
  - Basic features: S1G Beacon, NDP Control frame, TIM compression, Unified scaling factor for max idle pe- riod/listen interval/WNM-sleep interval, STA Type, S1G baseline functions (DCF, HCF, multi-rate support, A-MPDU), and S1G BSS operation
  - Network efficiency enhancements: PV1 frames, NDP PS-Poll/PS-Poll Ack/Probe Req./Probe Resp., RAW avoidance, TSBTT, and Differentiated EDCA Parameter
  - Power saving: Non-TIM operation, dynamic AID assignment, TWT, and Rescheduling STA's doze/awake cycle
  - Wider coverage: Relay
  - BSS scalability (up to 1024 STAs): Multicast AID, and Authentication control
  - Low-cost STA/AP: EL operation, Flow Control

- PHY
  - Full IEEE 802.11ah compatibility with enhanced performance
  - Single-stream up to 15Mbps data rate
  - Supports 1/2/4 MHz channel with optional SGI
  - Supports S1G_1M, Short/Long format
  - Support Traveling Pilot
  - Modulation: OFDM with BPSK, QPSK, 16QAM, 64QAM

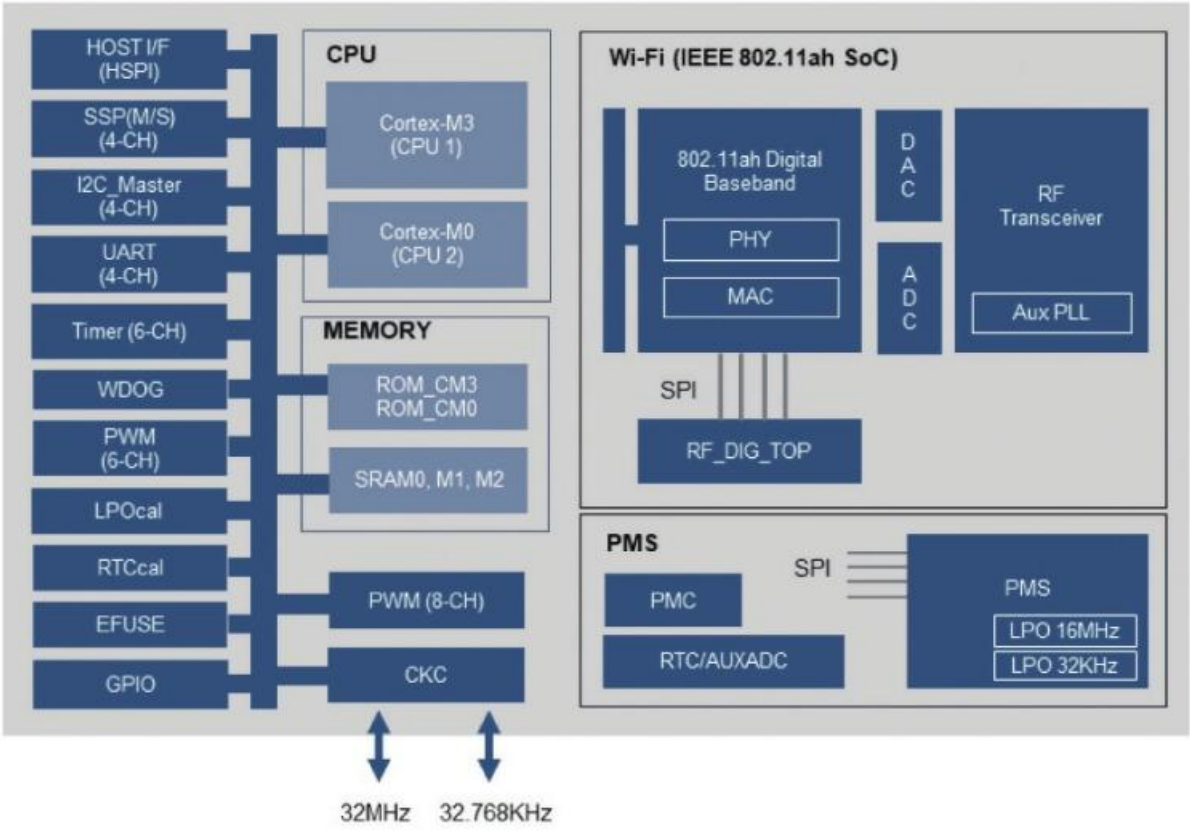
- BUS Sub-system

- Firmware code can be stored and executed in external Flash memory using XIP(execute-in-place) interface
- A few Wi-Fi dedicated digital blocks such as PMC for power management and RTC, UART for debug, a Wi-Fi dedicated HSPI for data transfer to host
- System Peripherals
  - 4 channel 32-bit timers
  - 2 channel 64-bit timers
  - 3 channel 32-bit Watchdog timers
  - XIP with cache (32KB cache memory)
- Data Peripherals
  - 5 pin HSPI(Host SPI) for host interface
  - General purpose I/Os
  - 4 channel SPIs master/slave
  - UART: 4 channel HSUARTs, up to 115200 baud rate
  - 4 channel I2C masters
  - PWM: 8ch
  - 9-bit ADC: 4ch

- RF transceiver
  - Based on the industry proven direct conversion transceiver architecture
  - Includes a complete radio front-end part, which consists of a pre-power amplifier and an LNA
  - Integrated LDOs
  - Wide supply voltage supportable with an integrated DC-DC buck converter
    - Usable battery voltage range: 2.1 ~ 3.6V
  - Radio calibration interfaces for digital baseband
    : TSSI, TX LOFT/IQ, RX IQ, LPF, PLL, BIAS current, SD-ADC
  - Fast AGC using built-in RSSI
  - Internal Temperature sensing and battery voltage monitoring
  - Single-ended RF port
  - Low supply current: RX 30mA @ 3.3V, TX 32mA @ 3.3V (0dBm Pout)
  - Frequency band: 750 ~ 950 MHz
  - Modulation bandwidth: 1/2/4 MHz
  - RX noise figure < 4dB
  - RX gain range: > 100dB
  - RX IIP3:-17dBm (@ LNA max. gain)
  - Linear output power: 0 dBm
  - TX gain range: > 30 dB
  - EVM <-34 dB @ 0dBm (w/ 64 QAM)
  - Integrated RF PLL phase error < 0.7 degree.

1.2 Block Diagram

Figure 1.1 illustrates ITM-6292N block diagram. ITM-6292N consists of Cortex-M3/M0 processors and a single BUS sub-system which can physically accommodate 802.11ah modem and many different types of peripherals.



2. Pinout and Signal Descriptions

2.1 Ball Map

ITM-6292N package is 268-ball CABGA and the ball-map is illustrated in Figure 2.1.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DVSS	GPRF_11_GAIN_05	GPRF_12_GAIN_06	GPRF_13_GAIN_07	GPRF_19_PA_EN	GPRF_18	TCK_SWCLK	TDI	GP_29	GP_28	GP_23	GP_22	EFUSE_VDDQ	PM_VBAT1	PM_18VO	PM_18VI	PM_GNDA	PM_11VO
B	GPRF_10_GAIN_04	DVSS	GPRF_14_GAIN_08	GPRF_15_GAIN_09	GPRF_21_ANT_SEL_B	GPRF_20_ANT_SEL	GP_31	TRSTN	GP_27	GP_26	GP_21	GP_20	LDO_CTRL	DVSS	PM_SUB	PM_nPOR	PM_GNDA	PM_CP
C	GPRF_07_GAIN_01	GPRF_09_GAIN_03	DVSS	GPRF_17_TX_EN	GPRF_16_LNA_EN	TMS_SWD	TDO	GP_30	GP_25	GP_24	GP_19	GP_18	RESETN	DVSS	PMU_CTRL	PM_ENSL	PM_GNDA	PM_VPP
D	GPRF_05_RXGAIN_L	GPRF_06_GAIN_00	GPRF_08_GAIN_02													PM_ENCP	PM_14VI_LDO	PM_LXFB
E	GPRF_03_RF_SCLK	GPRF_02_RF_CSn	GPRF_04_TXGAIN_L		DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS		PM_TSTIO	PM_PGNDA	PM_PGNDA
F	GPRF_01_RF_DOUT	GPRF_00_RF_DIN	DVSS		DVSS	DVDDE_33	DVDDE_33	DVSS	DVSS	DVSS	DVSS	DVDDE_GP18_GP31	DVDDE_18	DVSS		PM_TSTEN	PM_PGNDA	PM_LX
G	DVSS	DVSS	RF_TEN		DVSS	DVDDE_33	DVDDE_33	DVSS	DVSS	DVSS	DVSS	DVDDE_GP18_GP31	DVDDE_GP00_GP17	DVSS		PM_RESET	PM_PGNDA	PM_VBATT
H	RF_SUBGRD	IF_TIP	IF_TIN		DVSS	DVSS	DVSS					DVDDE_GP18_GP31	DVDDE_GP00_GP17	DVSS		GP_12	GP_14	GP_16
J	RF_14VI_TX	IF_TQP	IF_TQN		DVSS	DVSS	DVSS		DVDDC_11	DVDDC_11		DVDDE_JTAG	DVDDE_GP00_GP17	DVSS		GP_13	GP_15	GP_17
K	RF_GNDPPAOB	RF_GNDPPA	RF_MNO		DVSS	DVDDC_11	DVDDC_11		DVDDC_11	DVDDC_11		DVDDE_HSPI	DVDDE_HSPI	DVSS		GP_10	GP_09	GP_11
L	RFO	RF_GNDPPA	RF_GNDPPA		NC	NC	DVDDC_11					DVDDE_XIP	DVDDE_XIP	DVSS		GP_07_UART3_RX	GP_06_UART3_TX	GP_08
M	RF_GNDPPAOB	RF_GNDA	RF_R25K		NC	NC	DVDDC_11	DVDDC_11	DVDDC_11	DVDDC_11	DVSS	DVDDE_MODE	DVDDE_XIP	DVSS		GP_01_UART2_RX	GP_03	GP_05_UART0_RX
N	RF_GNDA	RF_SUB	NC		NC	NC	DVDDC_11	DVDDC_11	DVDDC_11	DVDDC_11	DVSS	DVSS	DVSS	DVSS		GP_00_UART2_TX	GP_02	GP_04_UART0_TX
P	RF_AXAD1	RF_AXAD2	RF_AXAD3		NC	NC	RF_GNDA	DVSS	RF_GNDA	DVSS	DVSS	T_MODE	MODE_00	DVSS		DVSS	HSPI_nCS	HSPI_CLK
R	RF_GNDA	RF_GNDA	RF_SUB													DVSS	HSPI_MISO	HSPI_MOSI
T	RFIP	RF_GNDA	RF_VCOT	RF_VBAT	RF_GNDA	RF_14VI_PLL	IF_RIP	IF_RIN	RF_GNDA	RF_GNDD	RF_GNDD	MODE_01	MODE_04	XIP_WP_B	XIP_MOSI	DVDDE_XTAL_18	DVSS	HSPI_EIRQ
U	RFIN	RF_GNDA	RF_GNDA	RF_GNDA	RF_GNDA	RF_GNDA	IF_RQP	IF_RQN	RF_GNDA	RF_GNDD	RF_GNDD	RF_AXPLLT	MODE_03	XIP_nCS	XIP_MISO	DVDDC_XTAL_11	XI	DVSS
V	RF_GNDA	RF_GNDA	RF_GNDA	RF_18V_A	RF_12V_D	RF_GNDA	RF_12V_A	RF_14VI_A	RF_GNDXOSC	RF_XIN	RF_XOUT	RF_GNDXOSC	MODE_02	XIP_NC	XIP_CLK	AVDD_XTAL_11	XOUT	DVSS

2.2 Signal Descriptions

PART	NAME	Ball #	I/O Type	Volt	DESCRIPTION
Test mode	TMODE	P12	DI	DVDDE_MODE	Chip Test, normal GND
Boot mode	MODE_00	P13	DI	DVDDE_MODE	SW Define (When ROM BOOT) 11: Internal SRAM BOOT
	MODE_01	T12	DI	DVDDE_MODE	
	MODE_02	V13	DI	DVDDE_MODE	0: ROM BOOT 1: XIP BOOT
	MODE_03	U13	DI	DVDDE_MODE	0: Cortex-M0 Master 1: Cortex-M3 Master
	MODE_04	T13	DI	DVDDE_MODE	0: Two CPU 1: One CPU
External Flash I/F	XIP_CLK	V15	DO	DVDDE_XIP	Clock
	XIP_MOSI	T15	DIO	DVDDE_XIP	Data Serial – SI , Quad – data[3]
	XIP_MISO	U15	DIO	DVDDE_XIP	Data Serial – SO, Quad – data[2]
	XIP_WP_B	T14	DIO	DVDDE_XIP	Data Serial – NC, Quad – data[1]
	XIP_NC	V14	DIO	DVDDE_XIP	Data Serial – NC, Quad – data[0]
	XIP_nCS	U14	DIO	DVDDE_XIP	Chip Select (active low)
32K Crystal	XO_32K	V17	DO	DVDDE_XTAL_18	32 kHz Crystal sense input
	XI_32K	U17	DI	DVDDE_XTAL_18	32 kHz Crystal sense output
HSPI	HSPI_EIRQ	T18	DO	DVDDE_HSPI	Host SPI – Interrupt
	HSPI_MOSI	R18	DI	DVDDE_HSPI	Host SPI – Master out Slave in
	HSPI_MISO	R17	DO	DVDDE_HSPI	Host SPI – Master in Slave out
	HSPI_nCS	P17	DI	DVDDE_HSPI	Host SPI – Chip Select (active low)
	HSPI_CLK	P18	DI	DVDDE_HSPI	Host SPI – Clock
GPIO	GP_00	N16	DO	DVDDE_GP00_GP17	UART Channel2 Tx
	GP_01	M16	DI	DVDDE_GP00_GP17	UART Channel2 Rx
	GP_02	N17	DO	DVDDE_GP00_GP17	UART Channel2 RTS
	GP_03	M17	DI	DVDDE_GP00_GP17	UART Channel2 CTS
	GP_04	N18	DO	DVDDE_GP00_GP17	UART Channel0 Tx
	GP_05	M18	DI	DVDDE_GP00_GP17	UART Channel0 Rx
	GP_06	L17	DO	DVDDE_GP00_GP17	UART Channel3 Tx
	GP_07	L16	DI	DVDDE_GP00_GP17	UART Channel3 Rx
	GP_08	L18	DIO	DVDDE_GP00_GP17	Multiple purpose

PART	NAME	Ball #	I/O Type	Volt	DESCRIPTION
					(GPIO,I2C,PWM,SPI, Ext-INT)
	GP_09	K17	DIO	DVDDE_GP00_GP17	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_10	K16	DIO	DVDDE_GP00_GP17	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_11	K18	DIO	DVDDE_GP00_GP17	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_12	H16	DIO	DVDDE_GP00_GP17	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_13	J16	DIO	DVDDE_GP00_GP17	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_14	H17	DIO	DVDDE_GP00_GP17	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_15	J17	DIO	DVDDE_GP00_GP17	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_16	H18	DIO	DVDDE_GP00_GP17	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_17	J18	DIO	DVDDE_GP00_GP17	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_18	C12	DIO	DVDDE_GP18_GP31	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_19	C11	DIO	DVDDE_GP18_GP31	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_20	B12	DIO	DVDDE_GP18_GP31	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_21	B11	DIO	DVDDE_GP18_GP31	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_22	A12	DIO	DVDDE_GP18_GP31	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_23	A11	DIO	DVDDE_GP18_GP31	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_24	C10	DIO	DVDDE_GP18_GP31	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_25	C9	DIO	DVDDE_GP18_GP31	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_26	B10	DIO	DVDDE_GP18_GP31	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_27	B9	DIO	DVDDE_GP18_GP31	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_28	A10	DIO	DVDDE_GP18_GP31	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_29	A9	DIO	DVDDE_GP18_GP31	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_30	C8	DIO	DVDDE_GP18_GP31	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)
	GP_31	B7	DIO	DVDDE_GP18_GP31	Multiple purpose (GPIO,I2C,PWM,SPI, Ext-INT)

PART	NAME	Ball #	I/O Type	Volt	DESCRIPTION
Reset	RSTn	C13	DI	DVDDE_18	Hardware reset input Connect this pin to PM_nPOR (B16)
PMS[2]	PM_VBATT	G18	PI	V_{BAT}	supply voltage (2.1~3.6V)
	PM_LX	F18	AO	1.45V	PWM output Connect this pin to an external L(15uH) C(10uF) filter
	PM_18VI	A16	PI	1.8V	Buck drive supply input Connect to PM_18VO
	PM_18VO	A15	PO	1.8V	Internal LDO output Connect a 4.7uF bypass Cap. between this pin and GND
	PM_VPP	C18	PO	V_{BAT}-1.8V	Internal LDO output, power supply input Connect a 2.2uF bypass Cap. between this pin and GND
	PM_LXFB	D18	AI	1.45V	Buck feedback voltage input
	PM_14VI_LDO	D17	PI	1.45V	1.1V LDO input.
	PM_CP	B18	AIO	1.45V	Buck compensation node Connect a series R(24K) C(3.9nF) from this pin to GND
	PM_11VO	A18	PO	1.1V	Internal LDO output Connect a 4.7uF bypass Cap. between this pin and GND
	PM_nPOR	B16	DO	1.8V	Power on reset pulse out Connect to RSTn(C13)
	PM_ENSL	C16	DI	1.8V	Sleep mode control input Connect to PMU_CTRL
	PM_ENCP	D16	DI	1.8V	Buck compensation input Normal GND
	PM_TSTIO	E16	DO	1.8V	PMS Test signal output Test purpose, normal NC
	PM_TSTEN	F16	DI	1.8V	PMS test mode enable Test purpose, normal GND
	PM_RESET	G16	DI	V_{BAT}	PMS reset input (active high, normal low) This pin is internally pulled down with 200K Ohm
	PM_VBAT1	A14	PI	V_{BAT}	supply voltage (2.1~3.6V)
	PM_GNDA	A17, B17, C17 (PMS analog ground)			
	PM_PGNDA	E17, E18, F17, G17 (PMS buck ground)			
	PM_VSUB	B15 (PMS p-substrate ground)			

PART	NAME	Ball #	I/O Type	Volt	DESCRIPTION
	PMU_CTRL	C15	DO	DVDDE_18	Connect to PM_EN SL (C16)
	LDO_CTRL	B13	DO	DVDDE_18	NC
	EFUSE_VDDQ	A13	PI	2.5V	EFUSE power supply voltage Only used for E-Fuse writing Left this pin open otherwise
JTAG & Debug	nTRST	B8	DIO	DVDDE_JTAG	Test reset
	TCK	A7	DIO	DVDDE_JTAG	Test clock
	TDI	A8	DIO	DVDDE_JTAG	Test data input
	TMS	C6	DIO	DVDDE_JTAG	Test mode selection
	TDO	C7	DIO	DVDDE_JTAG	Test data output
RF/ Digital	GPRF_21	B5	DO	DVDDE_33	RF_ANTSEL_B
	GPRF_20	B6	DO	DVDDE_33	RF_ANTSEL
	GPRF_19	A5	DO	DVDDE_33	RF_PA_EN
	GPRF_18	A6	DO	DVDDE_33	3.3V GPIO
	GPRF_17	C4	DO	DVDDE_33	3.3V GPIO
	GPRF_16	C5	DO	DVDDE_33	RF_EXTLNA_ON
	GPRF_15	B4	DIO	DVDDE_33	3.3V GPIO
	GPRF_14	B3	DIO	DVDDE_33	3.3V GPIO
	GPRF_13	A4	DIO	DVDDE_33	3.3V GPIO
	GPRF_12	A3	DIO	DVDDE_33	3.3V GPIO
	GPRF_11	A2	DIO	DVDDE_33	3.3V GPIO
	GPRF_10	B1	DIO	DVDDE_33	3.3V GPIO
	GPRF_09	C2	DIO	DVDDE_33	3.3V GPIO
	GPRF_08	D3	DIO	DVDDE_33	3.3V GPIO
	GPRF_07	C1	DIO	DVDDE_33	3.3V GPIO
	GPRF_06	D2	DIO	DVDDE_33	3.3V GPIO
	GPRF_05	D1	DIO	DVDDE_33	3.3V GPIO
	GPRF_04	E3	DIO	DVDDE_33	3.3V GPIO
	GPRF_03	E1	DIO	DVDDE_33	3.3V GPIO
	GPRF_02	E2	DIO	DVDDE_33	3.3V GPIO
	GPRF_01	F1	DIO	DVDDE_33	3.3V GPIO
	GPRF_00	F2	DIO	DVDDE_33	3.3V GPIO
RF/ Analog	RF_TEN	G3	DI	3.3V	RF test mode input Normal GND
	RF_MNO	K3	AO	1.2V	RF test signal output (Test purpose) Normal NC

PART	NAME	Ball #	I/O Type	Volt	DESCRIPTION
	RF_R25K	M3	AIO	1.2V	RF test point Normal NC
	IF_TIP	H2	AI	1.2V	In-phase TX analog input (+) [Test purpose] Normal NC
	IF_TIN	H3	AI	1.2V	In-phase TX analog input (-) [Test purpose] Normal NC
	IF_TQP	J2	AI	1.2V	Quad-phase TX analog input (+) [Test purpose] Normal NC
	IF_TQN	J3	AI	1.2V	Quad-phase TX analog input (-) [Test purpose] Normal NC
	RF_14VI_TX	J1	AI	1.45V	TX RF front-end supply input
	RFO	L1	AO	1.45V	TX output
	RF_AXAD1	P1	AI	1.2V	AUXADC input 1
	RF_AXAD2	P2	AI	1.2V	AUXADC input 2
	RF_AXAD3	P3	AI	1.2V	AUXADC input 3
	RFIP	T1	AI	1.2V	RX positive input
	RFIN	U1	AI	1.2V	RX negative input
	RF_VCOT	T3	AO	1.2V	VCO test signal output [Test purpose] Normal NC
	RF_VBAT	T4	PI	3.3V	RF supply input (2.1~3.6V)
	RF_18V_A	V4	AIO	1.8V	Internal LDO output, power supply input. Connect a 4.7uF bypass Cap. between this pin and GND
	RF_12V_D	V5	AIO	1.2V	Internal LDO output, power supply input Connect a 4.7uF bypass Cap. between this pin and GND
	RF_XIN	V10	AIO	1.2V	Crystal oscillator input
	RF_XOUT	V11	AIO	1.2V	Crystal oscillator output
	RF_14VI_PLL	T6	PI	1.45V	Internal LDO supply input
	RF_12V_A	V7	AIO	1.2V	Internal LDO output, power supply input, Connect a 4.7uF bypass Cap. between this pin and GND
	IF_RQN	U8	AO	1.2V	Quad-phase RX output (-) [Test purpose] Normal NC

PART	NAME	Ball #	I/O Type	Volt	DESCRIPTION
	IF_RQP	U7	AO	1.2V	Quad-phase RX output (+) [Test purpose] Normal NC
	IF_RIP	T7	AO	1.2V	In-phase RX output (+) [Test purpose] Normal NC
	IF_RIN	T8	AO	1.2V	In-phase RX output (-) [Test purpose] Normal NC
	RF_14VI_A	V8	PI	1.45V	Internal LDO supply input
	RF_AXPLLT	U12	DO	1.2V	AUXPLL test signal output [Test purpose] Normal NC
	RF_GNDA	M2, N1, P7, P9, R1, R2, T2, T5, T9, U2, U3, U4, U5, U6, U9, V1, V2, V3, V6 (RF/Analog ground)			
	RF_GNDD	T10, T11, U10, U11 (RF/Digital ground)			
	RF_PSUB	N2, R3 (p-substrate ground)			
	RF_GNDPPA	K2, L2, L3 (Power amplifier ground)			
	RF_GNDPPAOB	K1, M1			
	RF_SUBGRD	H1 (p-substrate guard ring between RF and SoC)			
	RF_GNDXOSC	V9, V12			
Digital GND	DVSS	A1, B2, C3, G1, G2, F3, B14, C14, P16, R16, T17, U18, V18, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, F5, F8, F11, F14, G5, G8, G11, G14, H5, H6, H7, H14, J5, J6, J7, J14, K5, K14, L14, M11, M14, N11, N12, N13, N14, P8, P10, P11, P14, F9, F10, G9, G10			
Digital VDD	DVDDE_18	F13 (1.8V IO VDD)			
	DVDDE_GP00_GP17	G13, H13, J13 (IO VDD for GP_00 to GP_17)			
	DVDDE_GP18_GP31	F12, G12, H12 (IO VDD for GP_18 to GP_31)			
	DVDDE_JTAG	J12 (IO VDD for JTAG)			
	DVDDE_HSPI	K12, K13 (IO VDD for HSPI)			
	DVDDE_XIP	L12, L13, M13 (IO VDD for External Flash I/F)			
	DVDDE_MODE	M12 (IO VDD for Boot mode)			
	DVDDC_11	J9, J10, K6, K7, K9, K10, L7, M7, M8, M9, M10, N7, N8, N9, N10 (1.1V IO VDD)			
	DVDDE_XTAL_18	T16 (1.8V XTAL VDD)			
	DVDDC_XTAL_11	U16 (1.1V XTAL VDD)			
	DVDDE_33	F6, F7, G6, G7 (3.3V IO VDD)			
Analog VDD	AVDD_XTAL_11	V16 (1.1V XTAL VDD)			
None Connect	NC	L5, L6, M5, M6, N3, N5, N6, P5, P6			

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
V_{BAT} and V_{IO}	-0.5		3.8	V
VIO – V_{BAT} (differential)			0	V
Digital Input	-0.5		V_{IO} + 0.5	V
RF pins	-0.5		2.1	V
Analog pins	-0.5		2.1	V
Storage temperature range ($T_{STORAGE}$)	-40		+125	°C
Electrostatic Discharge (HBM)			TBD	kV
Electrostatic Discharge (MM)			TBD	V
Electrostatic Discharge (CDM)			TBD	V

✓ NOTE : Stresses above those listed in Absolute Maximum Rating may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

Parameter	Conditions[(1) (2)]	Min	Typ	Max	Unit
V_{BAT}, V_{IO} (shorted to V_{BAT})	Direct battery connection	2.1	3.3	3.6	V
V_{BAT}, V_{IO} (shorted to V_{BAT})	Pre-regulated 2.1 V	1.89	2.1	2.31	V
Ambient operating temperature (T_A)		-40		85	°C
Maximum junction temperature		-40		125	°C

✓ (1) To ensure WLAN performance, ripple on the 2.1- to 3.3-V supply must be less than ±300 mV.
✓ (2) To ensure WLAN performance, ripple on the 1.8-V supply must be less than 2% (±40 mV).

3.3 Current Consumption

Parameter	Conditions	Min	Typ	Max	Unit
TX mode current	TX 802.11ah, Pout=0 dBm, (MCS7,4 MHz BW)		32		mA
RX mode current	RX 802.11ah, - 80dBm, (MCS7, 4 MHz BW)		32		mA
Deep Sleep mode current	Only always on block turned on		20		uA

✓ Note: Unless otherwise specified, TA.=27°C, VBAT= 3.6V, using internal PMU. Measurements are done at antenna port, which is directly connected to the device.

3.4 DC Electrical Characteristics

Table 3.4 DC Electrical Characteristics (IO, VDDIO = 3.3V)

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	Input High Voltage	2		3.6	V
V_{IL}	Input Low Voltage	-0.3		0.8	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	1.57	1.68	1.81	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	1.21	1.32	1.45	V
V_{OH}	Output High Voltage	2.4			V
V_{OL}	Output Low Voltage			0.4	V
I_{OH}	High Level Output Current @ V_{OH}(min)	13.4	26.5	45.0	mA
I_{OL}	Low Level Output Current @ V_{OL}(max)	8.5	12.9	17.4	mA

✓ Note: VDDcore = 1.1V, Temperature = 25°C

Table 3.5 DC Electrical Characteristics (IO, VDDIO = 2.5V)

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	Input High Voltage	1.7		3.6	V
V_{IL}	Input Low Voltage	-0.3		0.7	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	1.23	1.34	1.43	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	0.92	1.01	1.12	V
V_{OH}	Output High Voltage	1.7			V
V_{OL}	Output Low Voltage			0.7	V
I_{OH}	High Level Output Current @ V_{OH}(min)	9.3	18.6	32.5	mA
I_{OL}	Low Level Output Current @ V_{OL}(max)	9.9	16.5	24.1	mA

✓ Note: VDDcore = 1.1V, Temperature = 25°C

Table 3.6 DC Electrical Characteristics (IO, VDDIO = 1.8V)

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	Input High Voltage	1.17		3.6	V
V_{IL}	Input Low Voltage	-0.3		0.63	V
V_{T+}	Schmitt Trigger Low to High Threshold Point	0.93	1.02	1.11	V
V_{T-}	Schmitt Trigger High to Low Threshold Point	0.62	0.73	0.82	V
V_{OH}	Output High Voltage	1.35			V
V_{OL}	Output Low Voltage			0.45	V
I_{OH}	High Level Output Current @ V_{OH}(min)	3.4	8.2	15.9	mA
I_{OL}	Low Level Output Current @ V_{OL}(max)	4.6	8.2	13.0	mA

✓ Note: VDDcore = 1.1V, Temperature = 25°C

4. AC Specifications

4.1 HSPI Timing

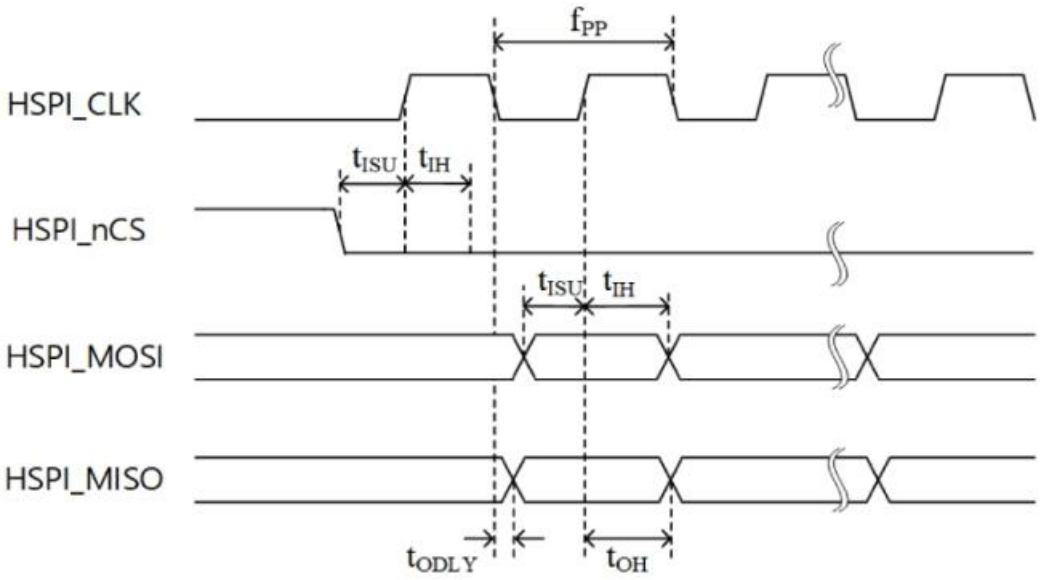


Table 4.1 AC Characteristic of HSPI

Symbol	Parameter	Min	Typ	Max	Unit
f_{PP}	Frequency	-	-	25	MHz
t_{ODLY}	Output delay time	6	-	-	ns
t_{OH}	Output hold time	2	-	-	ns
t_{ISU}	Input setup time	-	-	14	ns
t_{IH}	Input hold time	2.5	-	-	ns

4.2 SPI Timing

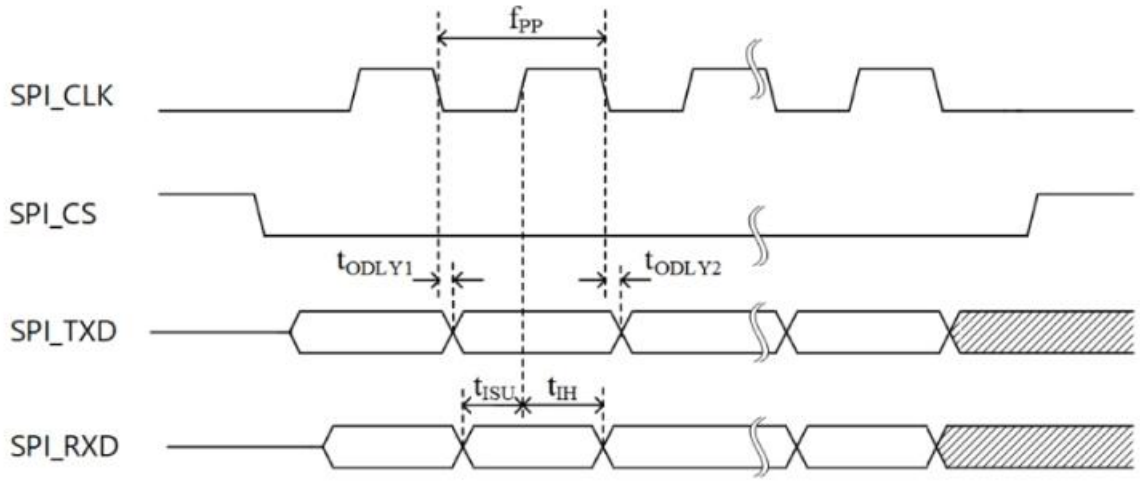


Table 4.2 SPI Timing Data

Symbol	Parameter		Min	Typ	Max	Unit
f_{PP}	Frequency	master	-	-	24	MHz
		slave	-	-	4	MHz
t_{ODLY1}	Output delay time1		0	-	10	ns
t_{ODLY2}	Output delay time2		0	-	10	ns
t_{ISU}	Input setup time		18	-	-	ns
t_{IH}	Input hold time		20	-	-	ns

4.3 XIP(eXecute In Place) Timing

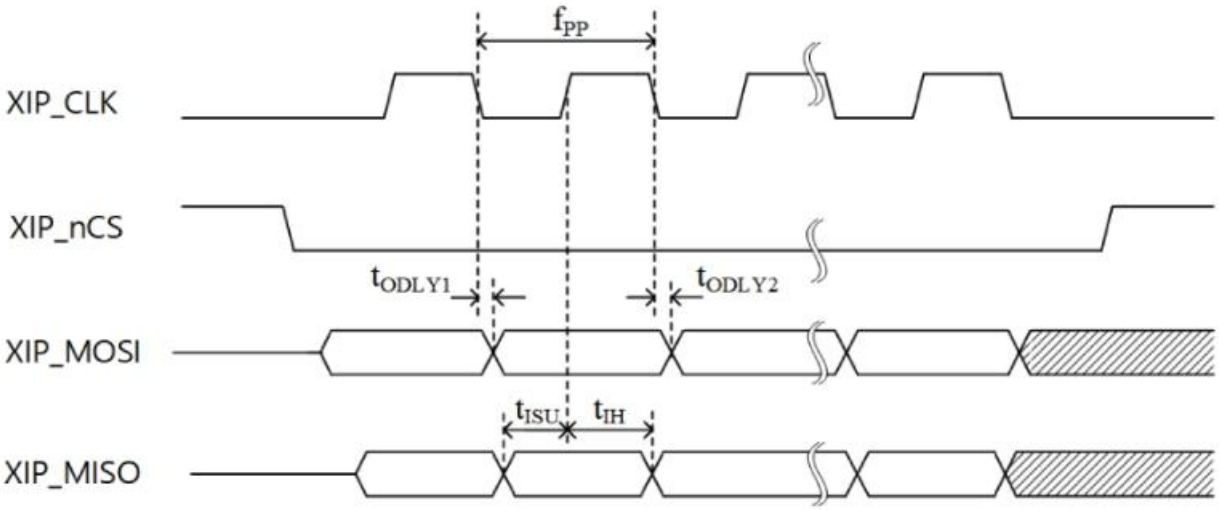


Table 4.3 XIP Timing Data

Symbol	Parameter	Min	Typ	Max	Unit
f_{PP}	Frequency	-	-	24	MHz
t_{ODLY1}	Output delay time1	0	-	15	ns
t_{ODLY2}	Output delay time2	0	-	15	ns
t_{ISU}	Input setup time	7	-	-	ns
t_{IH}	Input hold time	6	-	-	ns

4.4 AUXADC Timing

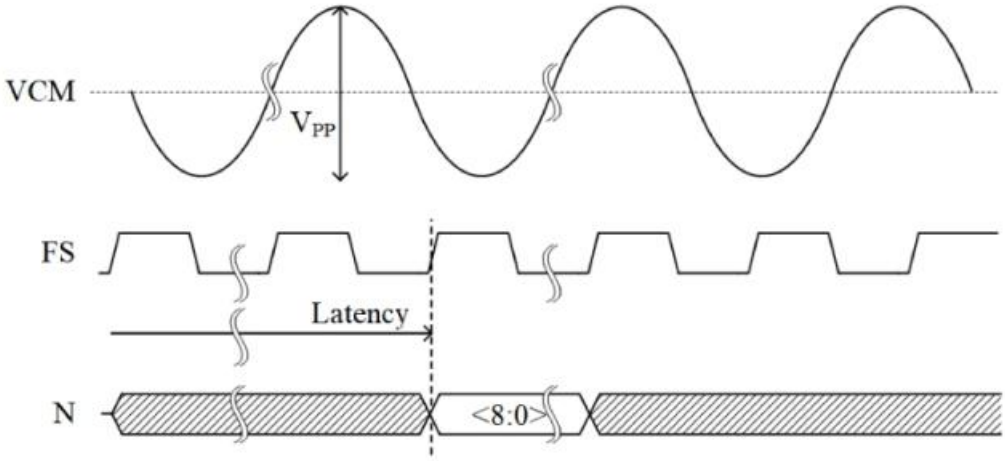


Table 4.4 AUXADC Timing Data

Symbol	Parameter	Min	Typ	Max	Unit
VCM	Input common-mode voltage	0.25	0.28	0.31	V
V_{PP}	Input Swing	-	0.5	-	Vpp
FS	Sampling Clock	-	32	-	MHz
Latency	Conversion latency(1 cycle = 31.25 ns)	-	11	-	cycle
N	Resolution	-	9	-	Bit
RIN	Input impedance	-	1	-	Mohms
I_active	Current consumption (1.2V supply)	-	-	300	uA
I_down	Power-down current (1.2V supply)	-	-	1	uA

5. 11ah WLAN RF Specifications and Performance

5.1 Transmitter Specifications

Parameter	Conditions[1] [2]	Min	Typ	Max	Unit
RF Output Frequency Range		750		950	MHz
EVM compliant output Output Power	150 kbps(MCS10, 1 MHz BW)		8		dBm
	13.5 Mbps (MCS7, 4 MHz BW)		5		dBm
EVM at 0 dBm output power		34	35	36	dB
Transmitter Spurious Signal Emissions	< 700 MHz		<-36		dBm/ MHz
	> 1 GHz		<-45		
RF Output Return Loss	Single ended output port		-10		dB
Output 1dB Gain Compression	1 MHz CW signal input		10		dBm
Gain Control Range		30			dB
Gain Control Step			1		dB
Unwanted Sideband	Over RF channel, RF frequency, and baseband frequency at 0 dBm output power		<-40		dBc
Baseband Filter Stop band rejection	At 96 MHz frequency offset		45		dB

✓ Note: Unless otherwise specified, TA.=27°C, VBAT=2.1 to 3.6V. RF input/outputs specifications are referenced to device pin and do not include 1dB loss from EV kit OCB and SMA connector. 100mVRMS sine and cosine signal (or 100mVRMS 54Mbp IEEE 802.11ah I/Q signals wherever OFDM is mentioned) applied to baseband I/Q input of transmitter (differential DC coupled).

5.2 Receiver Specifications

Parameter	Conditions[1] [2]	Min	Typ	Max	Unit
RF Input Frequency Range		750		950	MHz
RF Input Return Loss	For LNA high/mid/low gain modes	-10	-12	-15	dB
Total Voltage Gain Range	Analog + Digital Gain	-10		92	dB
RF Gain Step	From high gain mode to medium gain mode		6		dB
RX Gain Step	From RF to Analog		1		dB
DSB Noise Figure	LNA max gain mode		3.5		dB

Parameter	Conditions[1] [2]	Min	Typ	Max	Unit
IIP3	LNA with high gain mode		-17		dBm
	LNA with low gain mode		24		
Baseband Filters for Receiver (Analog + Digital Filter)					
Baseband -3dB Low-pass Corner Frequency (Controllable)	1 MHz channel		0.5		MHz
	2 MHz channel		1.0		MHz
	4 MHz channel		2.0		MHz

✓ Note: Unless otherwise specified, TA.=27°C, VBAT=2.1 to 3.6V. RF input/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit OCB and SMA connector.

5.3 Transmitter Performance

DR/MCS/BW (Mbps/ /MHz)	IEEE Relative constellation error (dB)	EVM (%) (IEEE)	EVM (%) (NRC_GGATE)	Comments
0.15/MCS10/1	-4	63.1	2.4	BPSK Peak
0.30/MCS0/1	-5	56.2	2.5	BPSK Peak
0.60/MCS1/1	-10	31.6	2.6	0 dBm OFDM, RMS
0.90/MCS2/1	-13	22.4	2.6	0 dBm OFDM, RMS
1.20/MCS3/1	-16	15.8	2.7	0 dBm OFDM, RMS
1.80/MCS4/1	-19	11.2	2.5	0 dBm OFDM, RMS
2.40/MCS5/1	-22	7.9	2.5	0 dBm OFDM, RMS
2.70/MCS6/1	-25	5.6	2.6	0 dBm OFDM, RMS
3.00/MCS7/1	-27	4.5	2.6	0 dBm OFDM, RMS
0.65/MCS0/2	-5	56.2	2.2	BPSK Peak
1.30/MCS1/2	-10	31.6	2.3	0 dBm OFDM, RMS
1.95/MCS2/2	-13	22.4	2.2	0 dBm OFDM, RMS
2.60/MCS3/2	-16	15.8	2.2	0 dBm OFDM, RMS
3.90/MCS4/2	-19	11.2	2.2	0 dBm OFDM, RMS
5.20/MCS5/2	-22	7.9	2.2	0 dBm OFDM, RMS
5.85/MCS6/2	-25	5.6	2.3	0 dBm OFDM, RMS
6.50/MCS7/2	-27	4.5	2.2	0 dBm OFDM, RMS
1.35/MCS0/4	-5	56.2	2.3	BPSK Peak
2.70/MCS1/4	-10	31.6	2.3	0 dBm OFDM, RMS
4.05/MCS2/4	-13	22.4	2.3	0 dBm OFDM, RMS
5.40/MCS3/4	-16	15.8	2.3	0 dBm OFDM, RMS
8.10/MCS4/4	-19	11.2	2.3	0 dBm OFDM, RMS
10.80/MCS5/4	-22	7.9	2.4	0 dBm OFDM, RMS
12.15/MCS6/4	-25	5.6	2.3	0 dBm OFDM, RMS
13.50/MCS7/4	-27	4.5	2.2	0 dBm OFDM, RMS

✓ Conditions: supply voltage VBAT=2.1 ~ 3.6V, Ta=25°C, signal within spectrum mask.

5.4 Receiver Performance

5.4.1 Receiver Sensitivity

Band	BW	Rate	Modulation/Coding Rate	Conditions/Conditions	Chip Port Specification [dBm]		
		kbps			Min	Typ	Max
750~950 MHz	1 MHz	300	BPSK 1/2	@ PER<10%, 256 bytes Full Operating Temperature; Full Battery Voltage Range; Load Z : 50 Ohms;		-106	
		600	QPSK 1/2			-104	
		900	QPSK 3/4			-101	
		1200	16QAM 1/2			-98	
		1800	16QAM 3/4			-95	
		2400	64QAM 2/3			-91	
		2700	64QAM 3/4			-89	
		3000	64QAM 5/6			-88	
		150	BPSK 1/2 rep. 2x			-109	
	2 MHz	650	BPSK 1/2	@ PER<10%, 256 bytes Full Operating Temperature; Full Battery Voltage Range; Load Z : 50 Ohms;		-103	
		1300	BPSK 3/4			-100	
		1950	QPSK 1/2			-97	
		2600	QPSK 3/4			-94	
		3900	16QAM 1/2			-91	
		5200	16QAM 3/4			-87	
		5850	64QAM 2/3			-85	
		6500	64QAM 3/4			-84	
	4 MHz	1350	BPSK 1/2	@ PER<10%, 256 bytes Full Operating Temperature; Full Battery Voltage Range; Load Z : 50 Ohms;		-100	
		2700	QPSK 1/2			-97	
		4050	QPSK 3/4			-94	
		5400	16QAM 1/2			-91	
		8100	16QAM 3/4			-88	
		10800	64QAM 2/3			-84	
		12150	64QAM 3/4			-82	
		13500	64QAM 5/6			-81	

✓ Assumption: NF=4[dB], Implementation Loss=2[dB].
✓ This is the measurement value with current NRWRACOM 11ah RF chip-set only (without an external SPDT).

5.4.2 Adjacent Channel Rejection (ACR)

Band	BW	Rate	Modulation/Coding Rate	Conditions/Conditions	ACR [dB]		
		kbps			Min	Typ	Max
750~950 MHz	1 MHz	300	BPSK 1/2	@ PER<10%, $P_{desired}$=$P_{sensitivty}$ + 3dB, $P_{interfere}$]@ N+1 channel		32	
		600	QPSK 1/2			30	
		900	QPSK 3/4			29	
		1200	16QAM 1/2			28	
		1800	16QAM 3/4			25	
		2400	64QAM 2/3			24	
		2700	64QAM 3/4			23	
		3000	64QAM 5/6			22	
		150	BPSK 1/2 rep. 2x			35	
	2 MHz	650	BPSK 1/2	@ PER<10%, $P_{desired}$=$P_{sensitivty}$ + 3dB, $P_{interfere}$]@ N+1 channel		30	
		1300	BPSK 3/4			28	
		1950	QPSK 1/2			27	
		2600	QPSK 3/4			26	
		3900	16QAM 1/2			23	
		5200	16QAM 3/4			21	
		5850	64QAM 2/3			19	
		6500	64QAM 3/4			17	
	4 MHz	1350	BPSK 1/2	@ PER<10%, $P_{desired}$=$P_{sensitivty}$ + 3dB, $P_{interfere}$]@ N+1 channel		28	
		2700	QPSK 1/2			26	
		4050	QPSK 3/4			25	
		5400	16QAM 1/2			23	
		8100	16QAM 3/4			20	
		10800	64QAM 2/3			18	
		12150	64QAM 3/4			15	
		13500	64QAM 5/6			12	

✓ Assumption: NF=4[dB], Implementation Loss=2[dB].
✓ This is the measurement value with current NRWRACOM 11ah RF chip-set only (without an external SPDT).

6. Functional Description

ITM-6292N has two ARM MCU processors, Cortex-M3 and Cortex-M0, and a single AHB BUS subsystem which can accommodate 802.11ah modem and plenty of peripherals on a single die.

It is recommended that ARM Cortex-M3 is designated for host subsystem and Cortex-M0 is for Wi-Fi subsys- tem but there is no limitation.

There are four bunches of internal SRAM and these memories are shared with both host and Wi-Fi sub-system so that user can maximize the internal memory utilization depending on operation scenario.

6.1 SoC Subsystem

6.1.1 ARM Cortex M3 CPU

The Cortex-M3 processor is a low-power processor that features low gate count, low interrupt latency, and low-cost debug. It is intended for deeply embedded applications that require fast interrupt response fea- tures. The processor implements the ARM architecture v7-M.

6.1.2 ARM Cortex M0 CPU

The Cortex-M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite inter- face and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processors.

6.1.3 Mailbox

ITM-6292N has the interrupt based mailbox for the message transfer between two processors. For both paths which are from Cortex-M3 to Cortex-M0 processor or from Cortex-M0 to Cortex-M3 processor, each mailbox has one 32x8 FIFO. IRQ_TX is the interrupt notice for message transmission complete. IRQ_RX is for message event arrival.

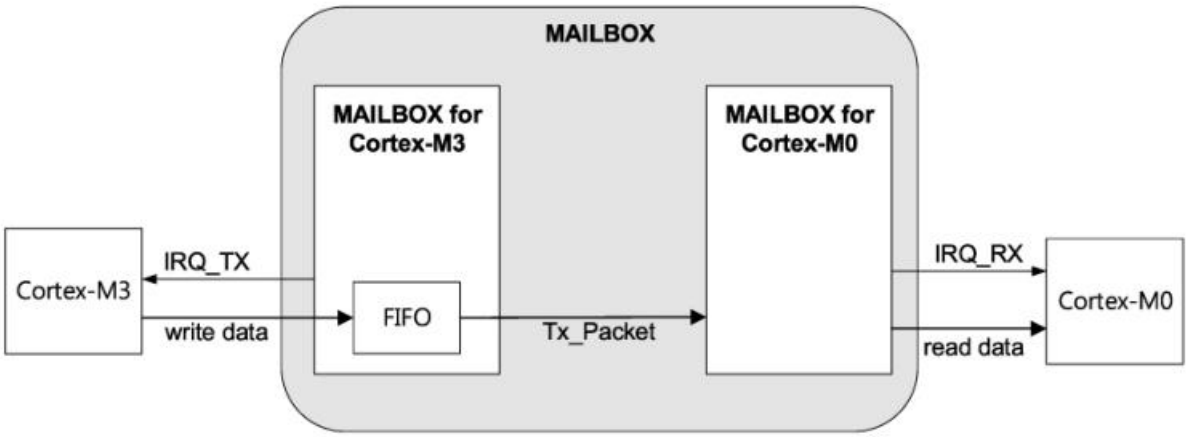


Figure 6.1 Mailbox Block Diagram (when Cortex-M3 sends a message)

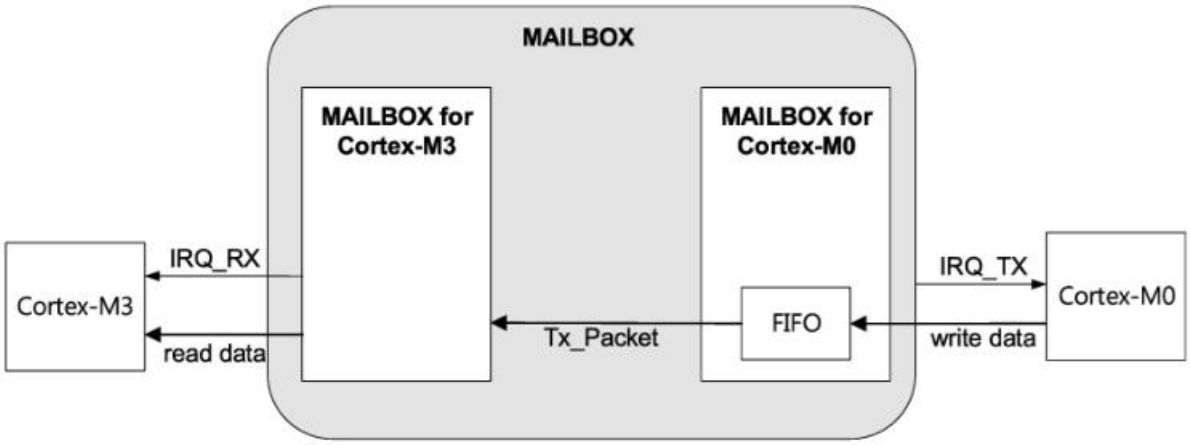
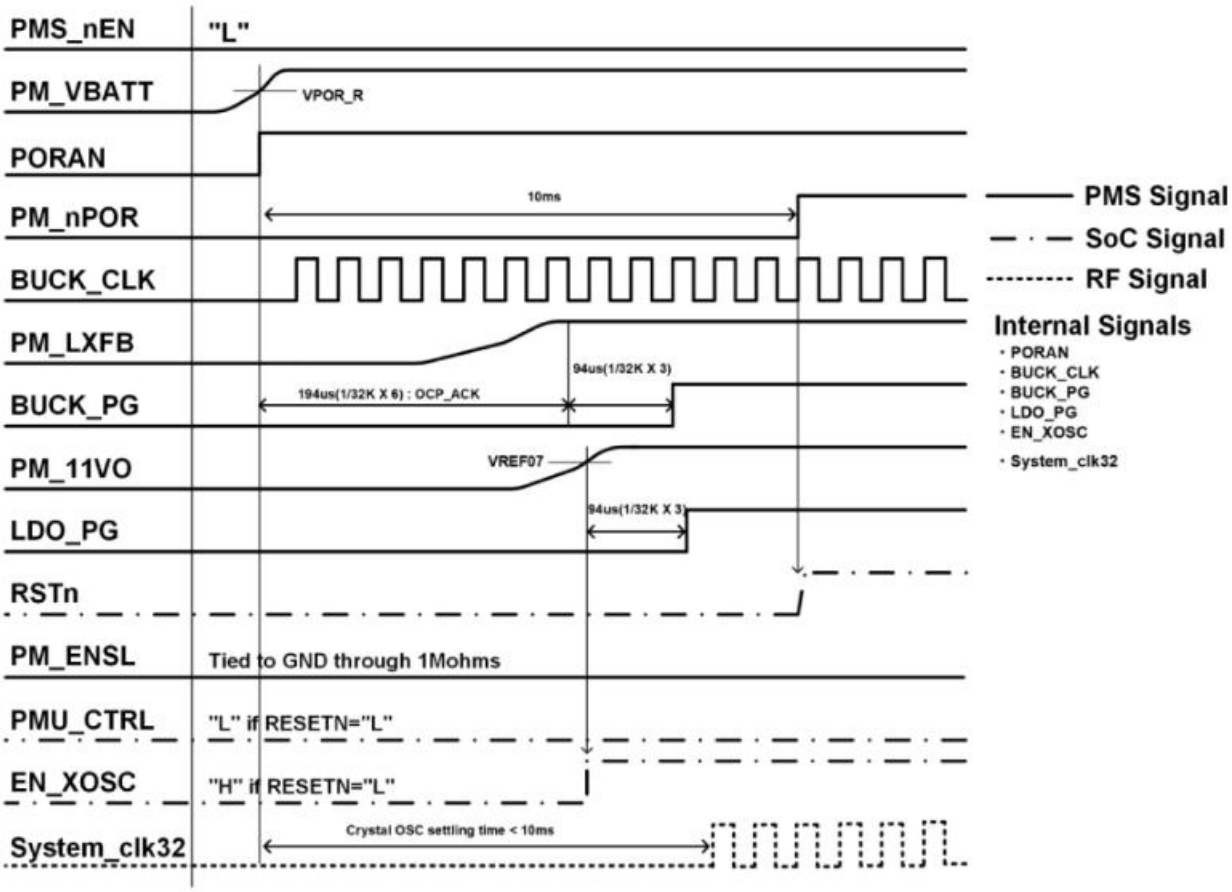


Figure 6.2 Mailbox Block Diagram (when Cortex-M0 sends a message)

6.1.4 Power on sequence

The sophisticated power on sequencer in ITM-6292N controls initial power-on procedure and power on re- set(PM_nPOR) as well.

A timing diagram of the power-on sequence is shown in Figure 6.3. The start of PM_nPOR circuit (PORAN) and BUCK oscillator are triggered by VBAT when its level is over the pre-defined voltage level. The main 32MHz crystal oscillator starts to run when the power supply is stable. The PM_nPOR (active low) is de-as- serted after pre-defined settling time for crystal oscillator to guarantee reliable SoC operation. When PM_ nPOR releases the RSTn (C13) to HIGH, the power-on sequence is finished and SoC can control the whole system.

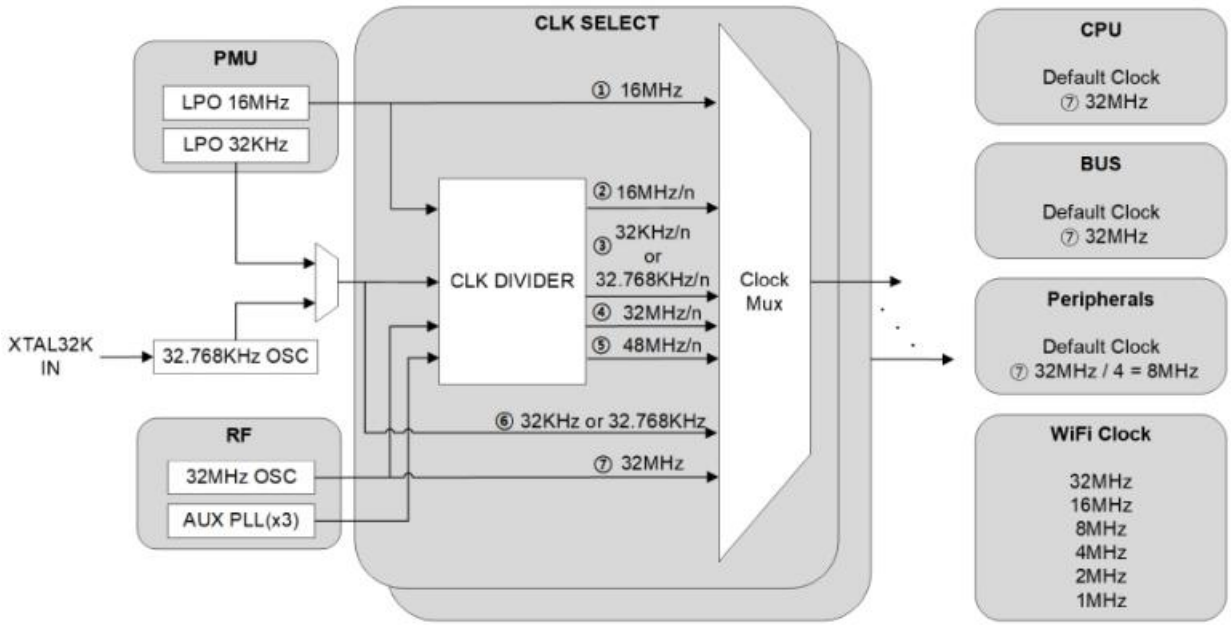


6.1.5 Clock

ITM-6292N has 5 primary clock source from two LPOs (16 MHz, 32 kHz), two XTALs (32.768 kHz, 32 MHz) and AUXPLL3. These clocks are used to generate the CPU clock, the bus clock and peripheral clocks. In addition, 32 kHz Low Power Oscillator (LPO) can be used instead of 32.768 kHz XTAL and 16 MHz LPO can also be used instead of 32 MHz XTAL.

32 MHz is the main source clock and this clock is used for CPU and BUS clock. The 32 kHz XTAL can be used for main clock for low power mode in order to reduce power consumption. The clock dividers and MUXs should be appropriately configured by software. The clock gating logic also can be configured by software to reduce power consumption during ACTIVE state. All the clock control registers can be configured dynamical- ly on BOOT and ACTIVE state.

There is calibrator controlled by PMU for 32 kHz LOP and this logic provides precise sleep clock to achieve lower power consumption in sleep mode. The 16 MHz LPO can be used when wake-up. This LPO runs only until the 32 MHz main XTAL is warmed up and stabled during wakeup or boot-up period. This procedure is automatically controlled by PMU.



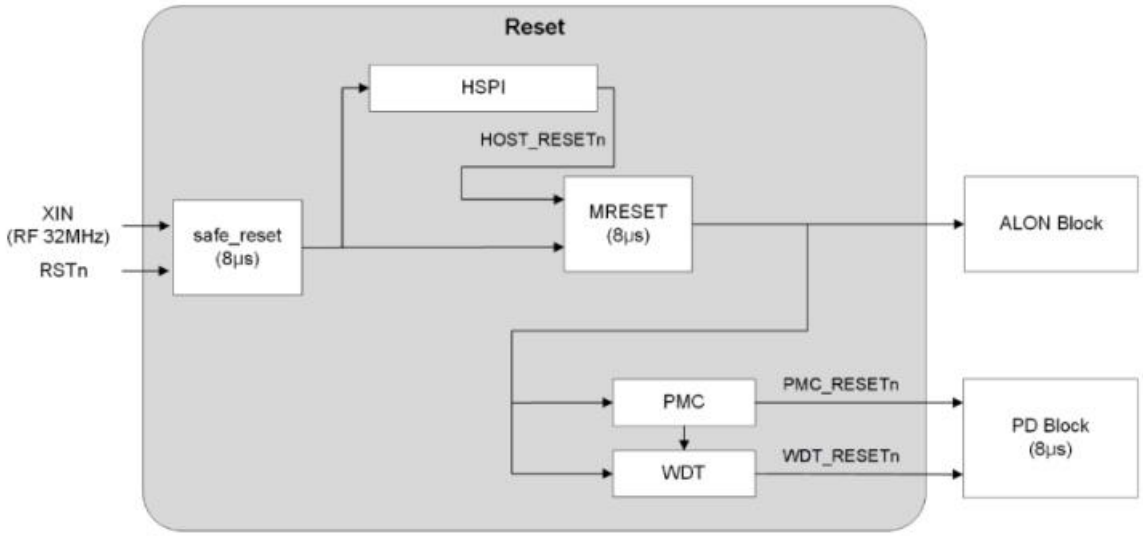
6.1.6 Reset

ITM-6292N has four global resets that is RSTn, HOST_RESETn, PMC_RESETn and WDT_RESETn. RSTn (C13) and HOST_RESETn can be used for system reset. PMC_RESETn and WDT_RESETn can reset all PD blocks in Figure 6.8, except ALON block.

Global RESET name	Source	Description
RSTn	External	ALON and PD Block
HOST_RESETn	Internal HSPI	ALON and PD Block
PMC_RESETn	Internal PMC	PD Block
WDT_RESETn	Internal WDT	PD Block

RSTn (C13) is the active low reset input. It contains a pull-up resistor and a glitch free circuit. More than 1us is recommended to assert reset to this pin.

Once it is asserted, the device is in reset state for about 24 us. External host also can reset ITM-6292N via HSPI interface.



6.1.7 Boot mode

The five ball pins are assigned as MODE[4:0] for boot mode selection so that ITM-6292N can provide flexible and configurable boot options as shown in Table 6.2.

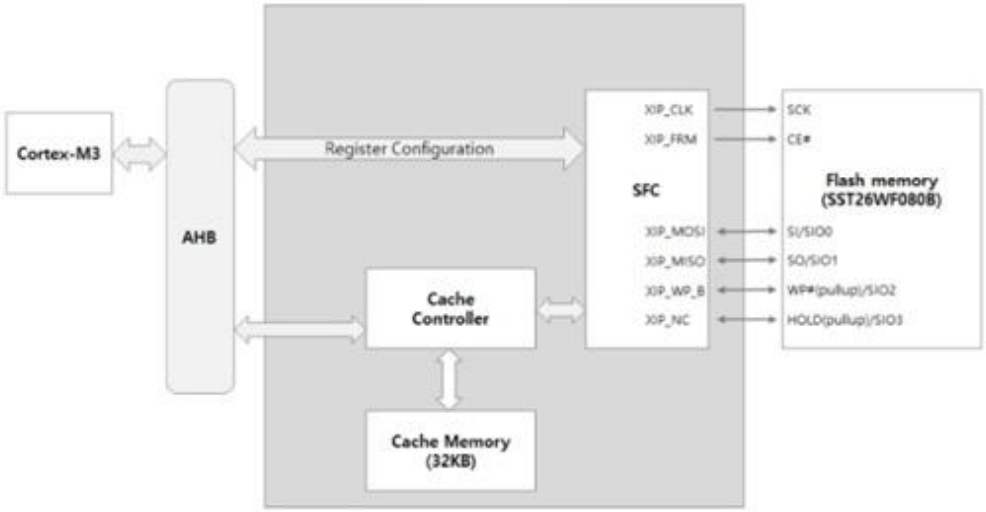
Especially in the case that the master CPU is Cortex-M3, XIP (eXecute-in-Place) using external Flash can be employed so that the size of code memory is not limited any more by the size of internal memory and flexi- bly it is expandable just to exchange external Flash memory.

MODE	Description
[4]	When 1, only one of two CPU processors boots up When 0, both of two CPU processors boot up sequentially
[3]	When 1, the Master CPU is Cortex-M3 When 0, the Master CPU is Cortex-M0
[2]	When 1, the start address for boot is remapped to the start address of XIP memory in physical memory map When 0, the start address for boot is remapped to the start address of ROM memory in physical memory map
[1:0]	When 2'b00, image download by mailbox between two CPU processors When 2'b01, image download via HSPI from Host When 2'b10, image download via UART3 from Host When 2'b11, firmware upgrade to external Flash memory via UART2

ITM-6292N can boot up with XIP mode when MODE[3:2] is '11'.. In this mode, other bits of the fields are don't care.

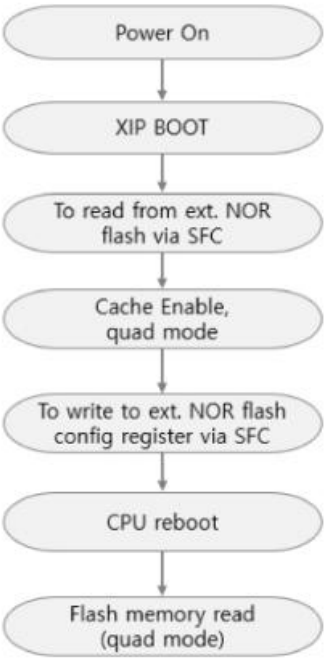
XIP block consists of a cache controller with 32KB cache memory, serial Flash controller that can communicate with external NOR flash memory. The cache controller is one-way and One cache line is 32byte so block has 1024 cache lines.

The power-on reset default of cache is disable.



Once XIP boot mode is selected, Cortex-M3 accesses XIP memory area as the remapped start address. Since the cache controller is bypass mode, SFC fetches the data from external flash memory with a single data read mode.

The initial firmware changes external flash operation mode to quad mode in order to enhance data speed and enable the cache controller for XIP. After XIP hardware configuration, CPU restarts for real XIP operation. The detail sequence is described at the flow chart in Figure 6.7.



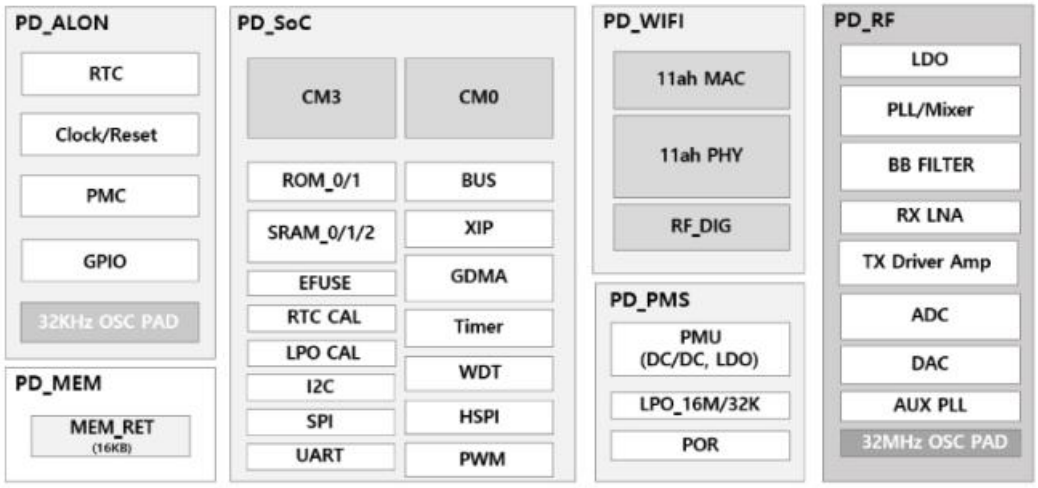
6.1.8 SCFG (System Configuration Register)

The SCFG define the operating modes of the ITM-6292N and its internal basic function like chip mode, remap, boot reason, and test clock configuration.

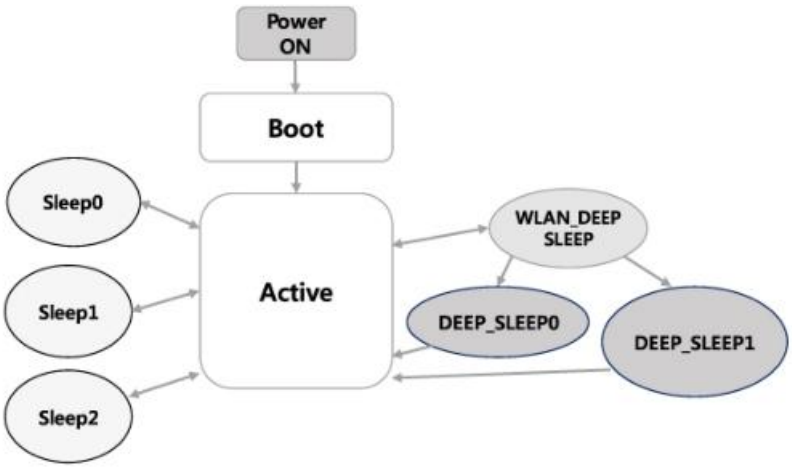
6.1.9 PMC (Power Management Controller)

PMC is the key controller block for power management of the ITM-6292N and controls power domain ON/OFF in accordance with each power state.

6.1.9.1 Power Domain and State



ITM-6292N consists of several power domains and is designed to provide various sleep mode options that us- ers can select depending on the scenario.

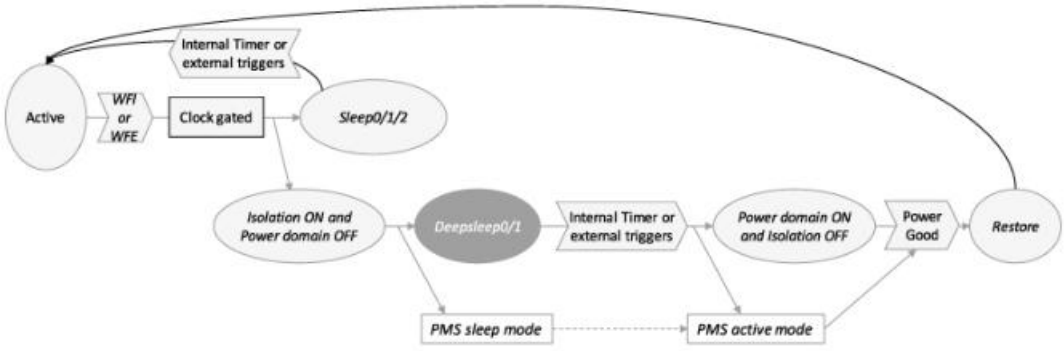


The PD_ALON is always-on block and designed to keep the minimum circuit turned on for fast wake up from the sleep mode upon wake-up event. The PD_SoC is the power domain turned on when Cortex-M0 or M3 is used and the PD_WIFI is power domain which can be power gated while Wi-Fi is not used. The PD_MEM is the power domain for retention memory. The retention memory can be used to store both code and data during sleep mode for fast wake up upon wake-up event. The other two, PD_RF and PD_PMS, are power do- main for RF transceiver and PMS, respectively.

In addition, there are six power states as shown in Table 6.3. This table represents on and off state of the clock and power in each power domain. The default power-on mode of ITM-6292N is active state.
The power consumption is decreased significantly by turning off main power-consuming domains in WLAN_ DEEP_SLEEP and two DEEP_SLEEP states. In three 'SLEEP' stats, clock gating is used to save power consump- tion. Except WLAN_DEEP_SLEEP state which is controlled by software, all other states are controlled by the PMC which provides highly efficient hardware control to minimize power consumption.

	SLEEP0	SLEEP1	SLEEP2	WLAN_ DEEPSLEEP	DEEP_ SLEEP0	DEEP_ SLEEP1
CPU/BUS	Clock OFF	Clock OFF	Clock OFF	ON	Power OFF	Power OFF
Internal Memory	Clock OFF	Clock OFF	Clock OFF	ON	Power OFF	Power OFF
All peripherals (except PMC/RTC)	Clock OFF	Clock OFF	Clock OFF	ON	Power OFF	Power OFF
Baseband	Clock OFF	Clock OFF	Clock OFF	Power OFF	Power OFF	Power OFF
Memory_RET	Clock OFF	Clock OFF	Clock OFF	ON	ON	ON
PMS	Active mode	Active mode	Active mode	Active mode	LP mode	LP mode
RF	Standby	Standby	Standby	Power OFF	Power OFF	Power OFF
32MHz OSC.	ON	OFF	OFF	ON	OFF	OFF
32kHz OSC. (w PMC/RTC)	ON	OFF	OFF	ON	ON	OFF

6.1.9.2 SLEEP/DEEP_SLEEP and Wakeup Procedure



Without any complicated manipulation, just executing 'WFI' or 'WFE' instruction with simple mode configuration, ITM-6292N can enter sleep state.

During ITM-6292N stays in a certain sleep state, only RTC timer interrupt, external host, or external GPIO can wake up the ITM-6292N . In DEEP_SLEEP state, only retention memory is powered on so that the important data required to be restored should be saved into retention memory before going into this state.

6.1.10 Memory

ITM-6292N includes the following memories and requires external Flash memory.

- ROM0/1
- SRAM0/1/2
- SRAM_RET for retention
- Two boot ROM for Cortex-M3 and Cortx-M0 respectively
- 32KB of cache memory for XIP

Cortex-M3/M0 ADDRESS MAP	Type	Device
32'h0000_0000 – 32'h0FFF_FFFF	Normal (write-through)	Start Address for Boot (ref. Boot mode)
32'h1010_0000 – 32'h1010_7FFF		Boot ROM for Cortex-M0 32KB
32'h1020_0000 – 32'h1020_7FFF		Boot ROM for Cortex-M3 32KB
32'h1040_0000 – 32'h1043_FFFF		SRAM0 256KB
32'h1044_0000 – 32'h1047_FFFF		SRAM1 256KB
32'h1048_0000 – 32'h104B_7FFF		SRAM2 224KB
32'h104B_8000 – 32'h104B_BFFF		SRAM_RET 16KB (with 16KB retention)
32'h1100_0000 – 32'h11FF_FFFF		XIP (Serial Flash Memory) 32MB
32'h2000_0000 – 32'h200F_FFFF	Normal (write-back write-allocate)	Reserved (Bit band region)
32'h2010_0000 – 32'h21FFF_FFFF		Reserved
32'h2200_0000 – 32'h230F_FFFF		Reserved (Bit band alias)

Cortex-M3/M0 ADDRESS MAP	Type	Device
32'h2400_0000 – 32'h3FFF_FFFF		Reserved
32'h4000_0000 – 32'h4000_0FFF	Device (APB0)	RTC
32'h4000_1000 – 32'h4000_1FFF		CKC
32'h4000_2000 – 32'h4000_2FFF		PMC
32'h4000_3000 – 32'h4000_3FFF		WDT(ADK)
32'h4000_4000 – 32'h4000_4FFF		TIMER-32(3 channel) TIMER-64(1 channel)
32'h4000_5000 – 32'h4000_5FFF		GPIO
32'h4000_6000 – 32'h4000_6FFF		I2C (4 channel)
32'h4000_7000 – 32'h4000_7FFF		SPI0
32'h4000_8000 – 32'h4000_8FFF		SPI1
32'h4000_9000 – 32'h4000_9FFF		UART0
32'h4000_A000 – 32'h4000_AFFF		UART1
32'h4000_B000 – 32'h4000_BFFF		SPI2 (for PMU control)
32'h4000_C000 – 32'h4000_CFFF		SPI3 (for RF control)
32'h4000_D000 – 32'h4000_DFFF		PWM (8 channel)
32'h4000_E000 – 32'h4000_EFFF		Reserved
32'h4000_F000 – 32'h4000_FFFF		SCFG
32'h4001_0000 – 32'h4003_FFFF	Device	Reserved
32'h4004_0000 – 32'h4004_0FFF	Device (APB1)	TIMER-32(1 channel) TIMER-64(1 channel)
32'h4004_1000 – 32'h4004_1FFF		UART2
32'h4004_2000 – 32'h4004_2FFF		UART3
32'h4004_3000 – 32'h4004_9FFF		Reserved
32'h4004_A000 – 32'h4004_AFFF		RTC CAL

Cortex-M3/M0 ADDRESS MAP	Type	Device
32'h4004_B000 – 32'h4004_BFFF		LPO CAL
32'h4004_C000 – 32'h4004_CFFF		AUXADC
32'h4004_D000 – 32'h4004_DFFF		EFUSE
32'h4004_E000 – 32'h4004_EFFF		Reserved
32'h4004_F000 – 32'h4004_FFFF		RF
32'h4005_0000 – 32'h4007_FFFF	Device	Reserved
32'h4008_0000 – 32'h4008_FFFF	Device (AHB)	WIFI
32'h4009_0000 – 32'h4009_0FFF		HSPI
32'h4009_1000 – 32'h4009_1FFF		DMA
32'h4009_2000 – 32'h4009_2FFF		SFC
32'h4009_3000 – 32'h4009_3FFF		MAILBOX
32'h4009_4000 – 32'h4FFF_FFFF	Device	Reserved
32'h5000_0000 – 32'h5009_3FFF	Device (Mirror region of 32'h4000_0000 – 32'h5009_3FFF)	Reserved
32'h5009_4000 – 32'h5FFF_FFFF	Device	Reserved
32'h6000_0000 – 32'h7FFF_FFFF	Normal (write-back write-allocate)	Reserved
32'h8000_0000 – 32'h9FFF_FFFF	Normal (write-through)	Reserved
32'hA000_0000 – 32'hDFFF_FFFF	External Device	Reserved
32'hE000_0000 – 32'hEFFF_FFFF	Reserved	Processor's internal peripherals
32'hF000_0000 – 32'hFFFF_FFFF	Device	None

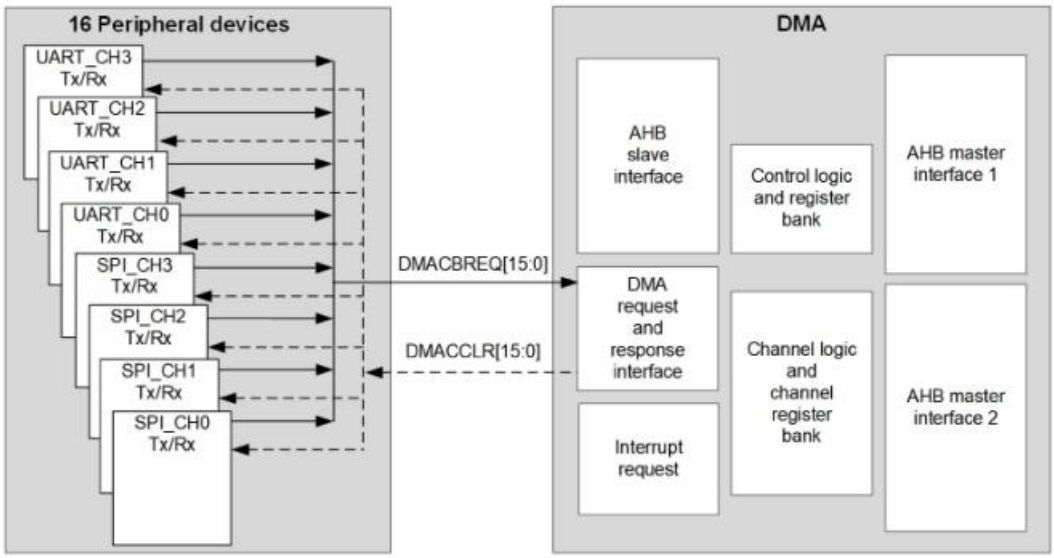
6.1.11 DMA

The DMA has 8 channels and each channel can be used for data transfer. The DMA offers 16 peripheral DMA request (DMACBREQ[15:0] or DMACSREQ[15:0]) and response (DMACCLR[15:0]) lines. These lines consist of 4 UART Tx, 4 UART Rx, 4 SPI Tx, and 4 SPI Rx. 16 peripheral devices connected with DMA are four UART channels and four SPI channels.

The DMA enables the following transactions

- Memory to Memory
- Memory to Peripheral
- Peripheral to Memory
- Peripheral to Peripheral

Each transfer type can have either the peripheral or the DMA as the flow controller, so there are eight possi- ble control scenarios.



6.1.12 RTC (Real-Time Clock)

RTC Timer is a specially designed 64-bit clock counter using 32.768 kHz clock with frequency offset compen- sation between RTC and main clock for accurate power management. This timer can be considered as the timer based autonomous trigger under system DEEP_SLEEP that the most logic blocks are powered off. It generates 'Interrupt' signal at the time when the preset time is over.

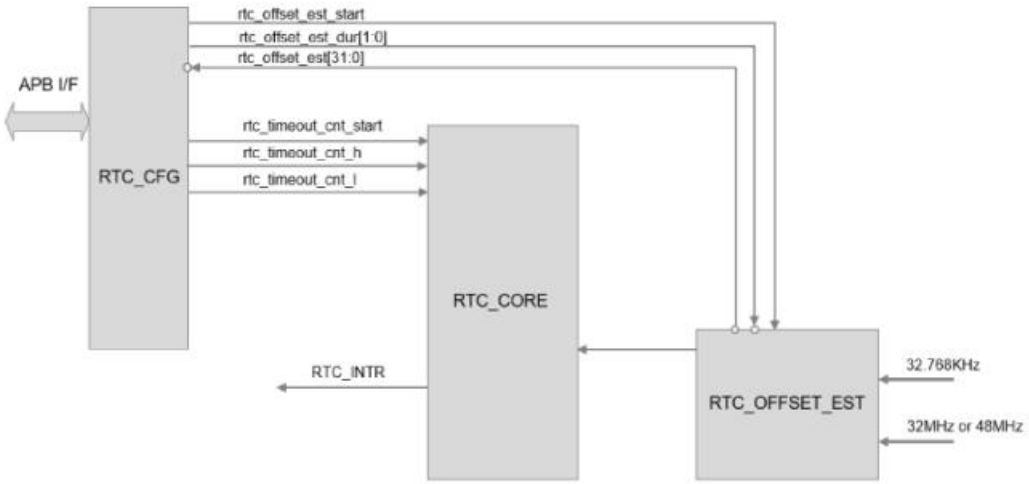
Inherently the low cost clock source such as crystal or crystal oscillator without temperature compensation has frequency instability as surrounding circumstances. The frequency offset estimation and compensation block are required to come over this disadvantage.

RTC timer supports two operation modes. One is countdown mode so called, bomb timer and the other is free running mode.

In countdown mode, the user sets the time duration and then enables the timer. The counter moves down until zero and generates interrupt immediately.

In free running mode, the user reads the current time and sets the desired future time. The interrupt is as- serted when the timer come to the preset time.

RTC Timer consists of RTC_CORE, RTC_CFG and RTC_OFFSET_EST.

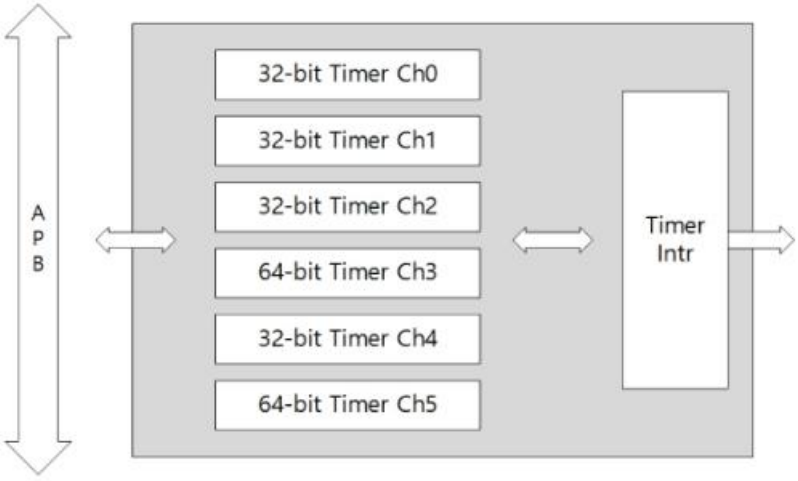


RTC_CFG is the bus interface for configuration and RTC_OFFSET_EST is the frequency offset estimation block which has the function to estimate the frequency difference between 32.768 kHz and 32 MHz reference clock in ppm.

RTC_CORE is the main clock counter block which is interrupt generator using RTC with the compensated clock frequency offset.

6.1.13 TIMER

This custom design timer consists of APB interface, four 32-bit timer, two 64-bit timer, and the interrupt log- ic. The timer is used to generate the interrupt at the specific time. After preset delay, it issues interrupt to the CPU. When using this timer, software overhead is minimal by the programmable hardware timer which can provide the variable length of delay.



Timer Features

- 4x 32-bit up-counter
- 2x 64-bit up-counter
- Each 32-bit prescaler per timer
- Supports the free-running mode and the one-shot mode

32bit Timer Channel number: Ch0, Ch1, Ch2, Ch4
64bit Timer Channel number: Ch3, Ch5

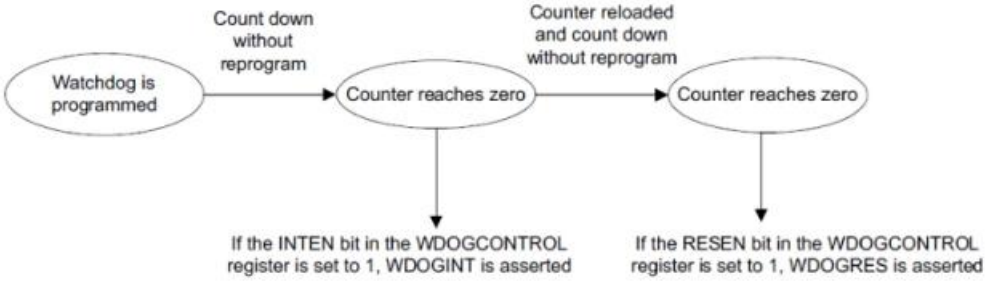
6.1.14 WDT (Watchdog Timer)

The watchdog applies a reset to a system in the event of a software failure, providing a way to recover from software crashes.

Designed the watchdog is based on a 32bit down-counter that is initialized from the Reload Register (WDO- GLOAD). The counter decrements by one on each rising edge of 32MHz reference clock when the clock en- able. (WDOGCLKEN is high)

The watchdog monitors the interrupt and asserts a reset request signal when the counter reaches 0, and the counter is stopped. On the next enable the counter is reloaded from the Reload Register and countdown sequence continues. If the interrupt is not cleared by the time the counter next reaches 0, the watchdog re- asserts the reset request signal.

The reset output is activated when the counter reaches 0 and the interrupt output is active, indicating that the counter has previously reached 0 but not been serviced.



6.1.15 EFUSE

ITM-6292N has internal 1024-bit one-time programmable electrical fuse (E-Fuse). It is used to store device specific configuration information like PMS and RF calibration parameters, MAC address and so on. E-fuse programming condition is defined as indicated in Table 6.5.

Condition.	EFUSE_VDDQ pin	Temp
E-Fuse WRITE	2.5V +/-10%	125 ~ -40
E-Fuse READ	0V or floating	125 ~ -40

6.1.16 INTERRUPT SOURCE

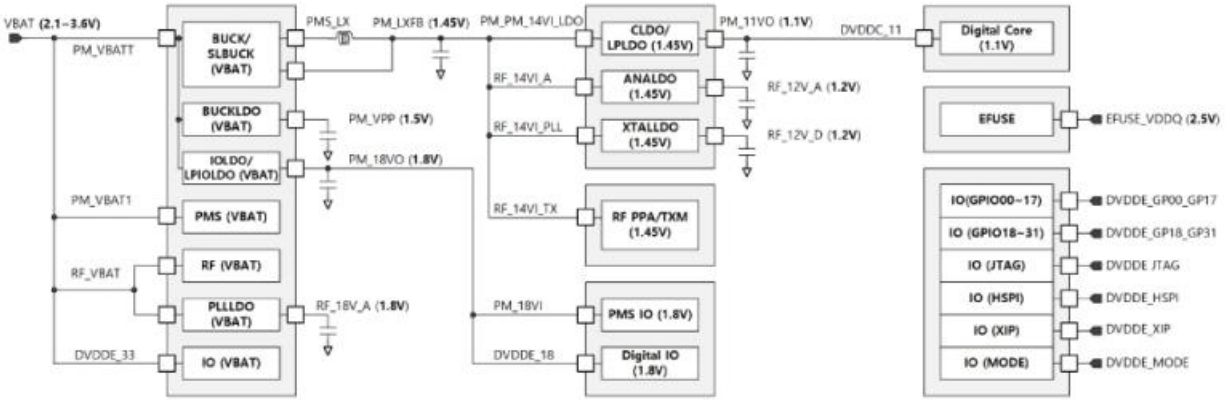
ITM-6292N has 16 inherent system interrupt sources and 32 user interrupt sources for two ARM Cortex-M3/ M0 processors, respectively.

No.	Exception Type / Source	Priority	Description	Note
1	Reset	-3 (Highest)	Reset	
2	NMI	-2	Non-Maskable Interrupt	
3	Hard Fault	-1	All fault conditions	

No.	Exception Type / Source	Priority	Description	Note
4	MemManageFault	Programmable	Memory management fault	Do not support
5	Bus Fault	Programmable	BUS Error	
6	Usage Fault	Programmable	Exception due to program error or trying to access co-processor	Do not support
7-10	Reserved	NA	-	
11	SVC	Programmable	Supervisor call	
12	Debug Monitor	Programmable	Debug monitor	
13	Reserved	NA	-	
14	PendSV	Programmable	Pendable service call	
15	SYSTICK	Programmable	System Tick Timer	
16	PMU	Programmable	PMU IRQ	0
17	TIMER4		TIMER4 IRQ	1
18	RTC		RTC IRQ	2
19	WDT		WDT IRQ	3
20	TIMER0		Timer0 IRQ	4
21	WIFI0		WIFI0 IRQ	5
22	DMACINTC		DMACINTTC	6
23	TIMER5		TIMER5 IRQ	7
24	TIMER1	Programmable	TIMER1 IRQ	8
25	UART0		UART0 IRQ	9
26	SPI0		SPI0 IRQ	10
27	PWR_FAIL		PWR_FAIL IRQ	11
28	LPO_INT		LPO_INT IRQ	12
29	DMACINTERR		DMACINTERR	13
30	-		-	14
31	UART3		UART3 IRQ	15
32	TIMER2	Programmable	TIMER2 IRQ	16
33	UART1		UART1 IRQ	17
34	SPI1		SPI1 IRQ	18
35	I2C		I2C IRQ	19
36	WIFI1		WIFI1 IRQ	20
37	WIFI2		WIFI2 IRQ	21
38	WIFI3		WIFI3 IRQ	22
39	-		-	23
40	TIMER3	Programmable	TIMER3 IRQ	24
41	UART2		UART1 IRQ	25
42	MAILBOX_Tx		MAILBOX_Tx IRQ	26
43	MAILBOX_Rx		MAILBOX_Rx IRQ	27
44	EXT0		EXT0 IRQ	28
45	EXT1		EXT1 IRQ	29
46	TXQUE		TXQUE IRQ	30
47	RXQUE		RXQUE IRQ	31

6.2 Power Management System

For low cost and highly power efficient system, the ITM-6292N integrates Brickcom proprietary Power Management System (PMS). The PMS integrates DC-DC BUCK converter and 6 LDOs as shown in Figure 6.15. Therefore, a single DC power range from 2.1 to 3.6V is required without any additional voltage regulator. For example, only two alkaline batteries can be enough as a single DC power supply.



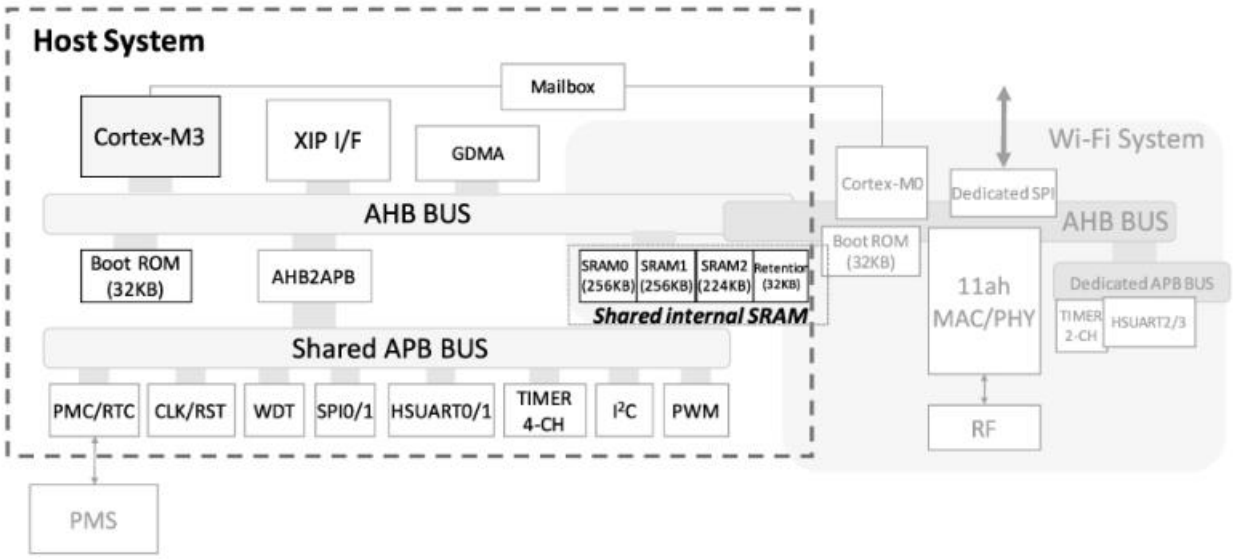
The BUCKLDO is designed for reliable BCUK switching operation. The three RF LDOs, PLLLDO, ANALDO, and XTALLDO, supply stable core voltage for PLL, RF and analog circuits, and crystal, respectively. The DC-DC con- verter is a high efficiency step-down converter and optimized by peak-current mode architecture with built- in synchronous power MOSFET switchers. The PMS contains additional features such as Soft Start, Over Cur- rent Protection (OCP). The DC-DC Converter generates a low ripple 1.45V for digital CLDO and RF LDOs with up to 100mA current.

To minimize sleep mode current, BUCK, IOLDO, and CLDO are switched to its sleep mode operation of SL-BUCK, LPIOLDO, and LPLDO, respectively.

The IOLDP generates regulated voltage for PMS IOs and Digital IOs. These are PM_ENSL (C16) and PM_ENCP (D16) and so on. The voltage level for external IO such as XIP and JTAG can be set by Digital VCC pins, DVD- DE_XIP and DVDDE_JTAG, respectively. This offers users flexibility in designing system interfaces. The EFUSE_ VDDQ is only used for writing internal eFuse macro in programming mode.

6.3 Modem System

6.3.1 Host System



To support extensive IoT applications, ITM-6292N provides various peripherals such as multi-channel UARTs, I2Cs, general SPIs and PWM, which enable to communicate with external sensor devices.

Preferably Cortex-M3 is used as a role of main host processor and has a dedicated 32KB boot ROM. The Cor- tex-M3 can manage power saving mainly by controlling PMC based on application scenarios.

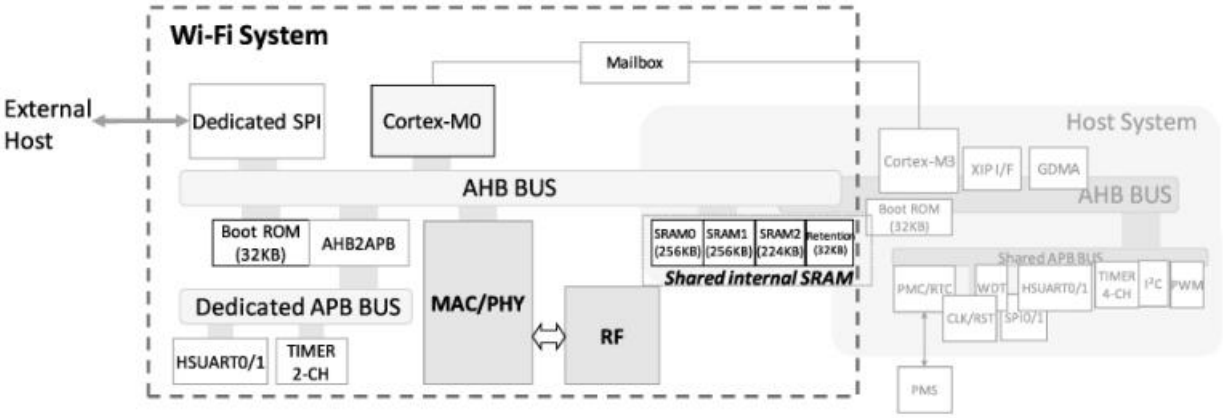
Even the system can be split logically into two systems but Cortex-M0 in the other side can access shared area, shared internal SRAM and shared peripherals if needed.

6.3.2 Wi-Fi System

Wi-Fi system includes a dedicated CPU to completely offload the host MCU along with an integrated radio and MAC/PHY with a powerful crypto engine. Even without any intervention of the host system, the CPU for Wi-Fi system can boot up independently with internal boot ROM by configuring boot mode.

To transfer control and data frame from/to host, the high speed HSPI is designated. In addition host can wake up from sleep/deep sleep and F/W download through this SPI as well.

Separating from the general APB peripherals, two UARTs and 64-bit Timers in the dedicated APB BUS can be assigned only for Wi-Fi operation.



6.3.3 Host system to Wi-Fi system communication

Both processors, Cortex-M0 and Cortex-M3, can exchange information via dedicated mailbox which is inter- rupt based mailbox.

7. Peripherals

ITM-6292N contains several peripherals to support system functions and offer interface for connection to the various devices. Please, refer to the following chapters.

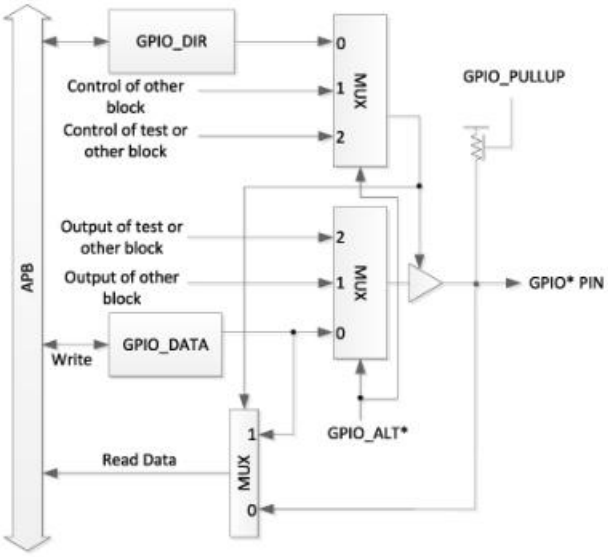
7.1 GPIO

ITM-6292N GPIO is a block that controls multi-function input/output and RF interface pins.

ITM-6292N includes

•32 GPIO pins (multi-functional input/output)

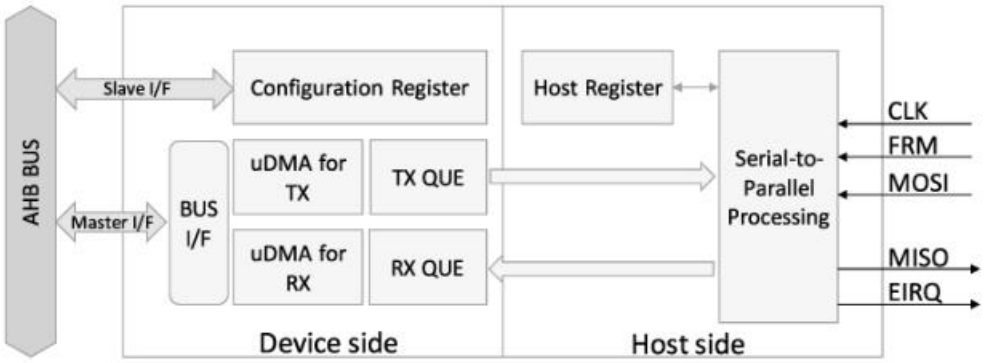
•22 GPIO pins for external RF interface pins



GPIO pins are shared and multiplexed with the signals from/to internal peripheral blocks include RF control. The multiplexing between GPIO mode and normal function mode (peripheral mode) is controlled by the state of the GPIO_ALT* register. If a bit of GPIO_ALT* is 1, the corresponding GPIO pin is configured in func- tion mode, and can be used by peripheral blocks instead of GPIO block.

7.2 HSPI

The block diagram of HSPI slave for a host interface is shown in Figure 7.2.



This SPI slave engine is customized building block to optimize control and management of host as well as in- crease speed of data transfer. It composes of two domains which are the host-side and the device-side. This separation can be used for power save operation. For example, when the device stays in deep sleep mode, most of blocks in the device can be powered down except host-side of HSPI and host can trigger system wake-up through host-side of HSPI.

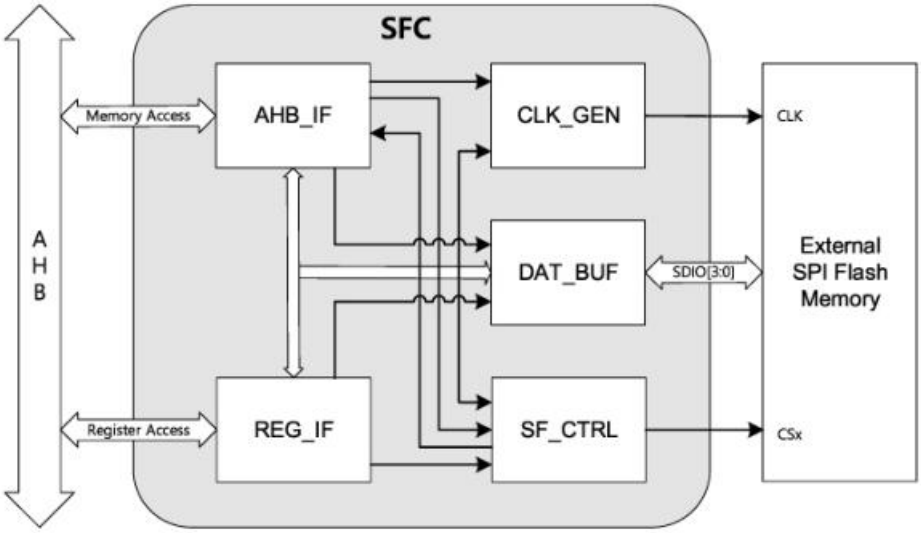
By using embedded micro DMA, this HSPI enables delivery of data from/to host without any other help from external processor or DMA.

With EIRQ interrupt, host can be informed about the device's status and easily manage data flow control. Total four types of programmable interrupt can be configured by resister.

7.3 SFC (Serial Flash Interface)

Flash Memory has a capacity limit of the 16 Mbytes memory. Its maximum operating speed of memory limited to 80 MHz and it is subject to AHB bus clock speed.

- support single, double and quad data transfer mode
- support flash erase / program for H/W and S/W
- support XIP(eXecute In Place)



7.4 I2C

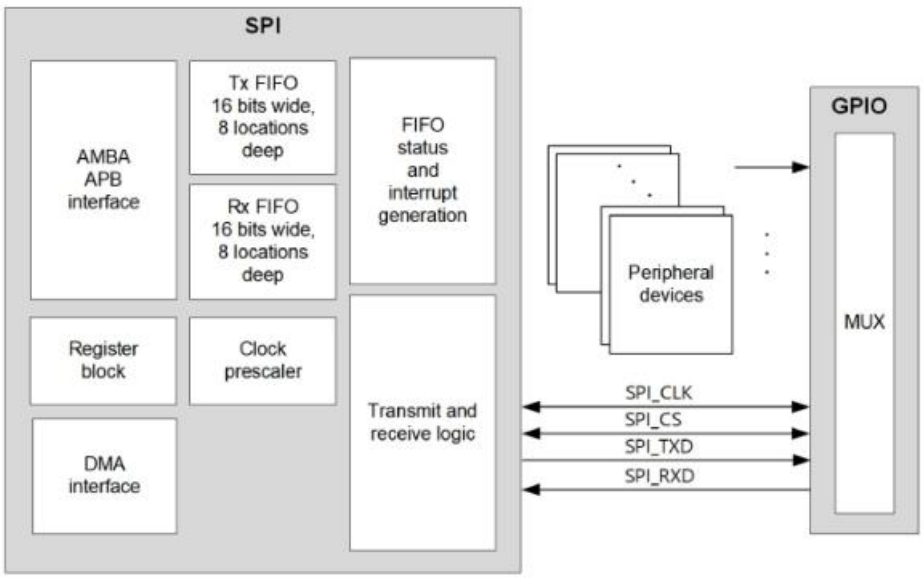
The I2C is a simple two-wire bus with a software-defined protocol. It supports 4 channels master mode in ITM-6292N.

7.5 SPI

ITM-6292N SPI has four channels. This SPI is a master or slave interface for synchronous serial communica- tion with peripheral devices that have Motorola SPI, National Semiconductor Microwire, or Texas Instru- ments synchronous serial interfaces.

The SPI performs serial-to-parallel conversion on data received from a peripheral device. The CPU accesses data, control, and status information through the AMBA APB interface. The transmit and receive paths are buffered with internal FIFO memories enabling up to eight 16-bit values to be stored independently in both transmit and receive modes.

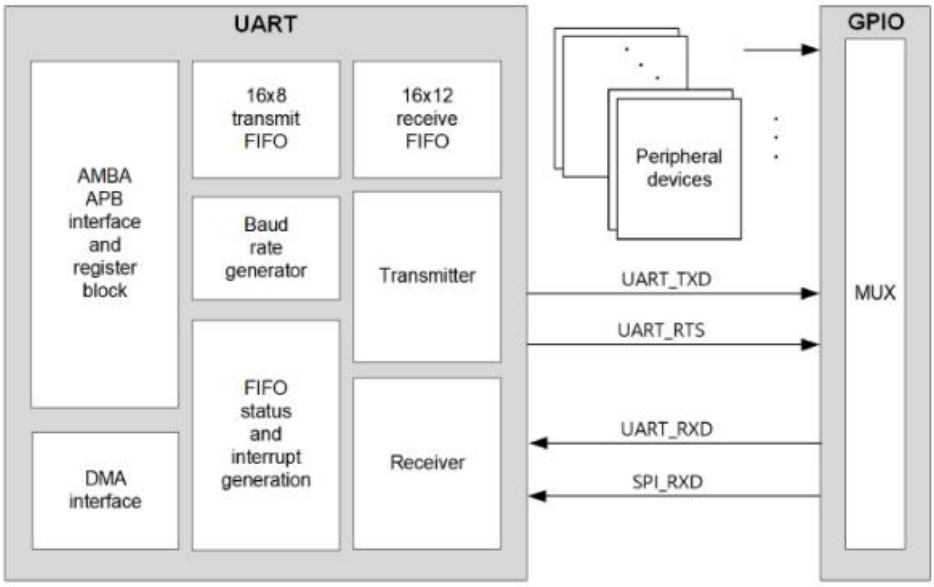
The SPI includes a programmable bit rate clock divider and prescaler to generate the serial output clock, SPI_CLK, from the input clock, SPI_PCLK.



7.6 UART

The UART is an AMBA slave module that connects to the Advanced Peripheral Bus (APB). The UART in- cludes an Infrared Data Association (IrDA) Serial InfraRed (SIR) protocol ENcoder/DECoder (ENDEC).

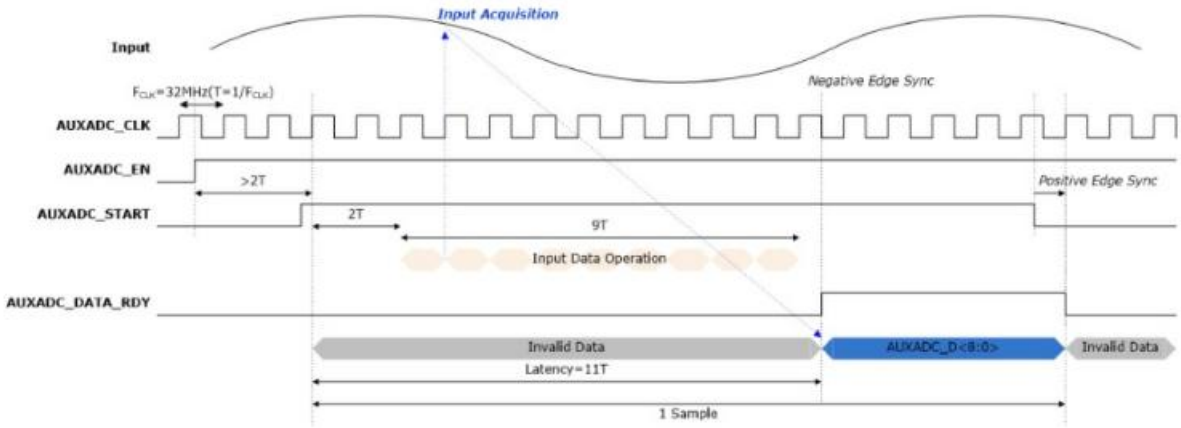
The CPU reads and writes data and control/status information through the AMBA APB interface. The trans- mit and receive paths are buffered with internal FIFO memories enabling up to 16-bytes to be stored inde- pendently in both transmit and receive modes.



7.7 PWM (Pulse Width Modulation)

There are four channels in the PWM module and four separate PWM blocks in one channel. Each PWM block can be programmed for an actuator driver or another device controlled by a PWM / PDM pulse.

7.8 AUXADC



ITM-6292N has 9-bits 4 channel auxiliary ADC for user application. Each channel can be selected with AUXA- DC_SEL in AUXADC register. Once it is enabled by AUXADC_EN in AUXADC register, the hardware automatically generates AUXADC_START signal about 2T after AUXADC_EN. Then, AUXADC_DATA_RDY signal is following it after about 9T. The AUXADC_DATA_RDY is connected to AUXADC_CHx_VALID flag in AUXADC register.

8. Mechanical Characteristics

Figure 8.1 Top and Side View of ITM-6292N Chip Package

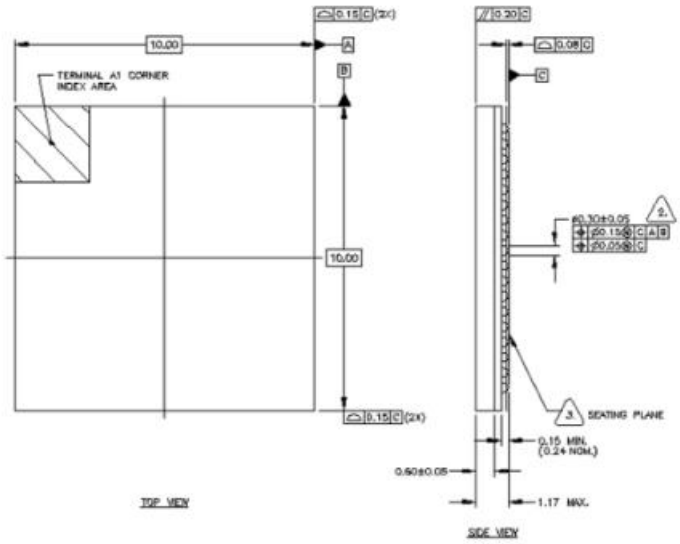
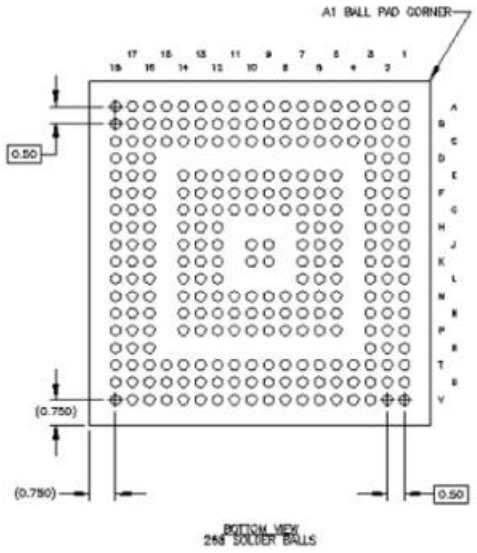


Figure 8.2 Bottom View of ITM-6292N Chip Package

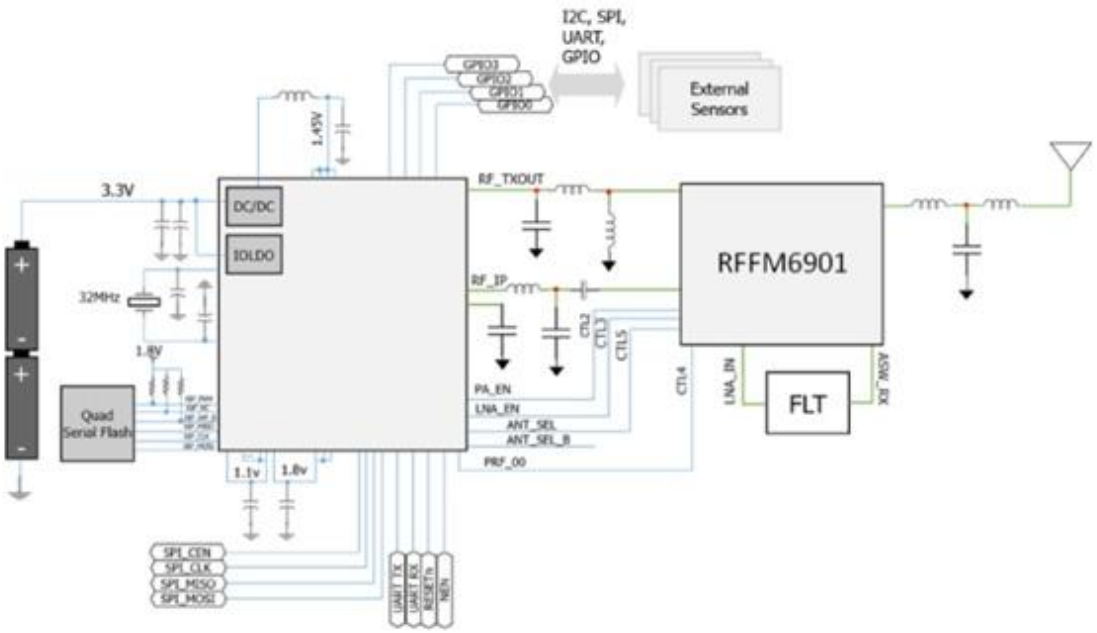


- Chip size : 100 mm2.
- Chip height: Typ. 1.14 mm, including the connecting bumps
- Package type: CABGA, 10x10, 268pin Package
- Ball Pitch: 0.5 mm. (Pitch)
- Ball Size: 0.3 mm
- Body size: Pb-free 10x10 mm

9. Application Circuit

ITM-6292N contains industry proven direct conversion RF transceiver including pre-amplifier. Its maximum output power is 0dBm. To increase output power, external front-end module (FEM) can be mounted as shown in *Quad Serial Flash : SST26WF080BT

Figure 9.1. In addition, external serial flash can be attached to increase memory for various applications.



10. Revision History

Revision No	Date	Comments
Ver 1.0	11/01/2018	Initial version for customer release created