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ITM-2075-02

ITM-2075-02

SiP module

(Preliminary)

V1.0

Revision History

Date	Revision Content	Revised By	Version
2022/09/20	- Initial released		1.0
	-		
	-		
	-		
	-		

Contents

1. FEATURES

MainChip:

IEEE 802.11ax compliant.

20/40/80 MHz channels for 5 GHz and 6 GHz radio, and 20 MHz channels for 2.4 GHz radio.

Full IEEE 802.11a/b/g/n/ac legacy. compatibility with enhanced performance.

Client MU-MIMO.

BT Core Specification Version 5.2, including the following support:

- Low energy (LE) isochronous channels
- LE power control
- LE enhanced connection update
- LE channel classification
- LE audio

Supports multiple simultaneous Advanced Audio Distribution Profiles (A2DP) for stereo sound.

Adaptive frequency hopping (AFH) to reduce radio frequency interference.

Supports battery range from 3.0V to 5.0V supplies with internal switching regulator.

Security:

WPA, WPA2 (Personal) with security improvements, and WPA3 (Personal) support for powerful encryption and authentication.

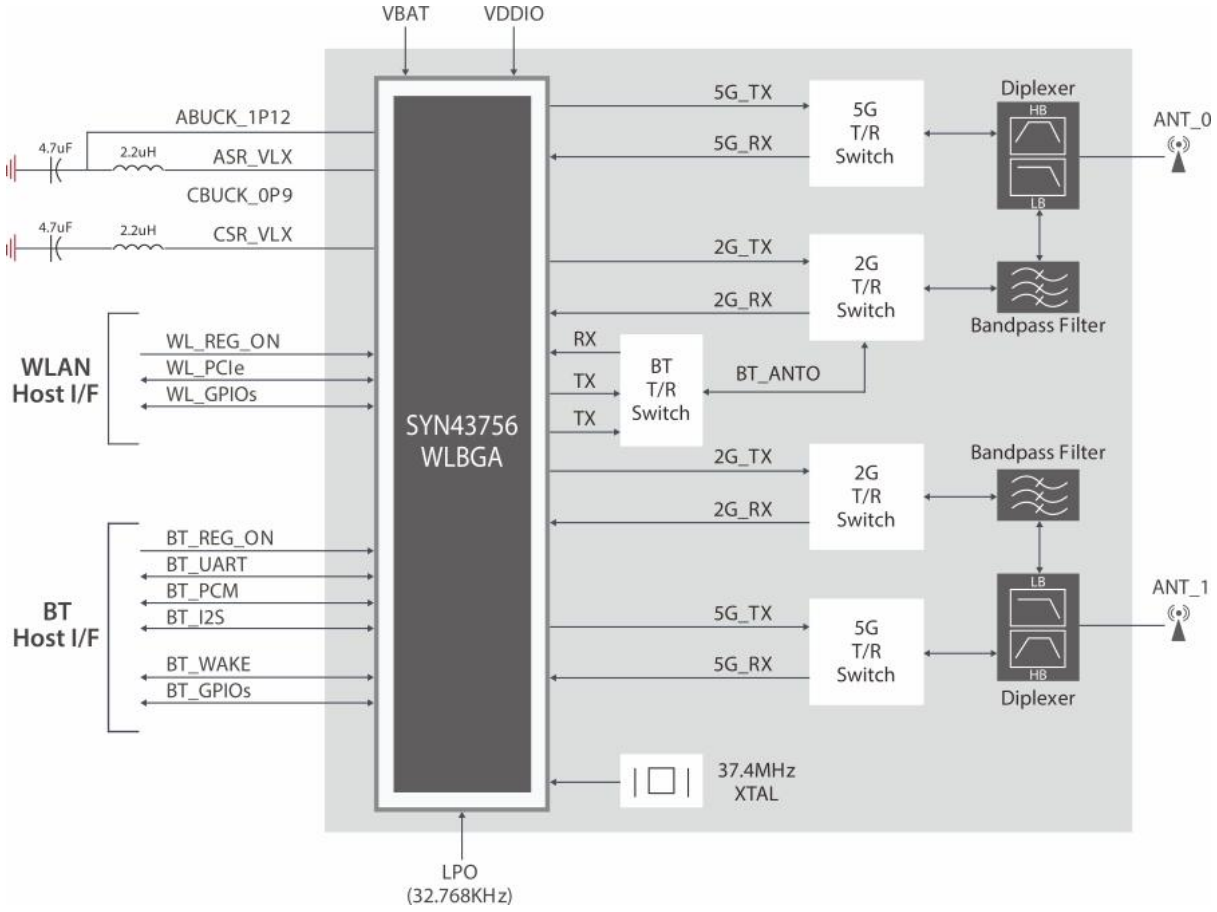
AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility.

Reference WLAN subsystem provides Wi-Fi Protected Setup (WPS)

Detail Specification:

Technical Specification	
MainChip	SYN43756
WiFi	Arm Cortex-R4
Bluetooth	5.1
Interface	WiFi: PCIe / BT: UART/PCM/I2S
Package	LGA-136pin
Moisture Sensitivity Levels(MSL)	Level-3
Dimension	10.0x10.0x0.982mm(Typ.)
Recommended Operation Conditions	
Operating Voltage	VBAT:3.2v ~ 4.8v / VDDIO:1.8v
Temperature	－30℃ ~ + 85℃
Humidity	Storage <60% / Operation <80%

2. BLOCK DIAGRAM



3. TECHNICAL SPECIFICATION

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Conditions	Min.	Nom.	Unit
VBAT	Main input supply from battery to switcher		-0.5	4.8	V
VDDIO	DC supply voltage for digital I/O		-0.5	2.07	V
ESD	Electro-static discharge voltage	HBM		TBD	KV
Ts	Storage temperature		-40	85	˚C
VBAT	Operating temperature		-30	85	˚C

RECOMMENDABLE OPERATION CONDITION

TEMPERATURE, HUMIDITY

Operating Temperature	-30° to +85° Celsius	
Relative Humidity range	Max 85%	Non condensing , relative humidity

VOLTAGE

Symbol	Parameter	Min	Typ.	Max	Unit
VBAT	Operation Voltage	3	3.6	4.8	V
VDDIO	DC supply voltage for digital I/O	1.62	1.8	1.98	V

CURRENT CONSUMPTION *(WLAN)*

Condition	Bandwidth(MHz)	Band(GHz)	Vbat=3.6V	VDDIO=1.8V	Unit
Off and Sleep Modes					
Off	-	-	0	0.01	mA
Sleep	-	-	0.08	0.09	mA
Active Transmit					
CCK 1 chain	20	2.4	525	5.8	mA
MCS8, Nss 1, HT20	20	2.4	240	4.2	mA
MCS7, HT20	20	5	361	4.5	mA
MCS7, HT40	40	5	340	3.6	mA
MCS8, Nss 1, VHT20	20	5	284	4.2	mA
MCS9, Nss 1, VHT40	40	5	210	3.6	mA

Condition	Bandwidth(MHz)	Band(GHz)	Vbat=3.6V	VDDIO=1.8V	Unit
MCS9, Nss 1, VHT80	80	5	274	3.3	mA
MCS11, Nss 1, HE20	80	5	308	2	mA
MCS11, Nss 1, HE40	40	5	200	2	mA
MCS11, Nss 1, HE80	80	5	210	1.6	mA
Active Receive					
1 Mbps, 1 RX core	20	2.4	57.4	0.91	mA
MCS7, HT20 1 RX core	20	2.4	59.8	0.91	mA
MCS7, HT20 1 RX core	20	5	68.1	1.21	mA
MCS7, HT20 2 RX core	20	5	86.2	1.3	mA
MCS7, HT40 1 RX core	40	5	73.1	1.2	mA
MCS7, HT40 2 RX core	40	5	97	1.28	mA
MCS9, Nss 1 , VHT80 1 RX core	80	5	83.5	1.19	mA
MCS9, Nss 1 , VHT80 2 RX cores	80	5	109.9	1.27	mA
MCS11, Nss 1, HE80 1 RX core	80	5	84.9	0.9	mA
MCS11, Nss 1, HE80 2 RX core	80	5	124.5	1.2	mA

CURRENT CONSUMPTION *(Bluetooth)*

Operating Mode	VBAT(3.6V)	VDDIO(1.8V)	Unit
Sleep Mode	40	75	uA
DM1/DH1	60	0.32	mA
DM3/DH3	110	0.34	mA
DM5/DH5	125	0.35	mA
BLE 1M	100	0.43	mA
BLE 2M	60	0.43	mA
Continue Rx Power	17	0.31	mA

WIRELESS SPECIFICATIONS

Features	Description
WLAN Standards	IEEE 802 Part 11a/b/g/n/ac (802.11a/b/g/n/ac/ax)
Bluetooth	Bluetooth TM 5.1compliance
Frequency Band	2.4 to 2.472GHz (1 to 13 channels)
	4.9 to 5.845GHz

RADIO SPECIFICATIONS 802.11A/B/G/N/AC

802.11B TRANSMIT

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	1~11Mbps	-	19		dBm
Transmit center frequency tolerance		-25	-	25	ppm
Transmit spectral mask	@+/-11MHz	-		-30	dBr
	@+/-22MHz	-		-50	dBr

802.11G TRANSMIT

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	6Mbps	-	19		dBm
Target Output Power Level	54Mbps	-	17		dBm
Transmit center frequency tolerance		-25	-	25	ppm
Transmit Modulation Accuracy	6Mbps		-	-5	dB
(EVM)	54Mbps			-25	dB
Transmit Spectral Mask	@+/-11MHz			-20	dBr
	@+/-20MHz			-28	dBr
	@+/-30MHz			-40	dBr

4GHZ 802.11N TRANSMIT – HT20

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	MCS0	-	19		dBm
Target Output Power Level	MCS7	-	16		dBm
Transmit center frequency tolerance		-25	-	25	ppm
Transmit Modulation Accuracy (EVM)	MCS0	-	-	-5	dB
	MCS7	-	-	-27	dB
Transmit Spectral Mask	@+/-11MHz	-		-20	dBr
	@+/-20MHz	-		-28	dBr
	@+/-30MHz	-		-45	dBr

4GHZ 802.11AC TRANSMIT – VHT20

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	MCS0	-	19		dBm
Target Output Power Level	MCS8	-	15		dBm
Transmit center frequency tolerance		-25	-	25	ppm
Transmit Modulation Accuracy (EVM)	MCS0	-	-	-5	dB
	MCS8	-	-	-30	dB
Transmit Spectral Mask	@+/-10.25MHz	-		-20	dBr
	@+/-20MHz	-		-28	dBr
	@+/-30MHz	-		-40	dBr

4GHZ 802.11AX TRANSMIT – HE20

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	MCS0	-	19	-	dBm
Target Output Power Level	MCS9	-	14	-	dBm
Transmit center frequency tolerance		-25	-	25	ppm
Transmit Modulation Accuracy (EVM)	MCS0	-	-	-5	dB
	MCS9	-	-	-32	dB
Transmit Spectral Mask	@+/-10.25MHz	-		-20	dBr
	@+/-20MHz	-		-28	dBr
	@+/-30MHz	-		-40	dBr

5GHZ 802.11A TRANSMIT

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	6Mbps	-	18	-	dBm
Target Output Power Level	54Mbps	-	16	-	dBm
Transmit center frequency tolerance		-20	-	20	ppm
Transmit Modulation Accuracy (EVM)	6Mbps	-	-	-5	dB
	54Mbps	-	-	-25	dB
Transmit Spectral Mask	@+/-11MHz	-	-	-20	dBr
	@+/-20MHz	-	-	-28	dBr
	@+/-30MHz	-	-	-40	dBr

5GHZ 802.11N TRANSMIT – HT20

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	MCS0	-	17	-	dBm
Target Output Power Level	MCS7	-	15	-	dBm
Transmit center frequency tolerance		-20	-	20	ppm
Transmit Modulation Accuracy (EVM)	MCS0	-	-	-5	dB
	MCS7	-	-	-27	dB
Transmit Spectral Mask	@+/-10.25MHz	-	-	-20	dBr
	@+/-20MHz	-	-	-28	dBr
	@+/-30MHz	-	-	-40	dBr

5GHZ 802.11N TRANSMIT – HT40

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	MCS0	-	17	-	dBm
Target Output Power Level	MCS7	-	14	-	dBm
Transmit center frequency tolerance		-20	-	20	ppm
Transmit Modulation Accuracy (EVM)	MCS0	-	-	-5	dB
	MCS7	-	-	-27	dB
Transmit Spectral Mask	@+/-20.5MHz	-	-	-20	dBr
	@+/-40MHz	-	-	-28	dBr
	@+/-60MHz	-	-	-40	dBr

5GHZ 802.11AC TRANSMIT – VHT20

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	MCS0	-	16	-	dBm
Target Output Power Level	MCS8	-	13	-	dBm
Transmit center frequency tolerance		-20	-	20	ppm
Transmit Modulation Accuracy (EVM)	MCS0			-5	dB
	MCS8	-	-	-30	dB
Transmit Spectral Mask	@+/-10.25MHz	-	-	-20	dBr
	@+/-20MHz	-	-	-28	dBr
	@+/-30MHz	-	-	-40	dBr

5GHZ 802.11AC TRANSMIT – VHT40

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	MCS0	-	17	-	dBm
Target Output Power Level	MCS9	-	14	-	dBm
Transmit center frequency tolerance		-20	-	20	ppm
Transmit Modulation Accuracy (EVM)	MCS0		-	-5	dB
	MCS9		-	-32	dB
Transmit Spectral Mask	@+/-20.5MHz	-	-	-20	dBr
	@+/-40MHz	-	-	-28	dBr
	@+/-60MHz	-	-	-40	dBr

5GHZ 802.11AC TRANSMIT – VHT80

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	MCS0	-	17	-	dBm
Target Output Power Level	MCS9	-	12	-	dBm
Transmit center frequency tolerance		-20	-	20	ppm
Transmit Modulation Accuracy (EVM)	MCS0		-	-5	dB
	MCS9		-	-32	dB
Transmit Spectral Mask	@+/-40.5MHz	-	-	-20	dBr
	@+/-80MHz	-	-	-28	dBr
	@+/-120MHz	-	-	-40	dBr

5GHZ 802.11AX TRANSMIT – HE20

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	MCS0	-	17	-	dBm
Target Output Power Level	MCS11	-	10	-	dBm
Transmit center frequency tolerance		-20	-	20	ppm
Transmit Modulation Accuracy (EVM)	MCS0		-	-5	dB
	MCS11		-	-35	dB
Transmit Spectral Mask	@+/-10.5MHz	-	-	-20	dBr
	@+/-40MHz	-	-	-28	dBr
	@+/-60MHz	-	-	-40	dBr

5GHZ 802.11AX TRANSMIT – HE40

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	MCS0	-	17	-	dBm
Target Output Power Level	MCS11	-	10	-	dBm
Transmit center frequency tolerance		-20	-	20	ppm
Transmit Modulation Accuracy (EVM)	MCS0		-	-5	dB
	MCS11		-	-35	dB
Transmit Spectral Mask	@+/-20.5MHz	-	-	-20	dBr
	@+/-40MHz	-	-	-28	dBr
	@+/-60MHz	-	-	-40	dBr

5GHZ 802.11AX TRANSMIT – HE80

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	MCS0	-	17	-	dBm
Target Output Power Level	MCS11	-	9	-	dBm
Transmit center frequency tolerance		-20	-	20	ppm
Transmit Modulation Accuracy (EVM)	MCS0		-	-5	dB
	MCS11		-	-35	dB
Transmit Spectral Mask	@+/-40.5MHz	-	-	-20	dBr
	@+/-80MHz	-	-	-28	dBr
	@+/-160MHz	-	-	-40	dBr

6GHz 802.11AX TRANSMIT

Item	Condition	Min.	Typ.	Max.	Unit
Target Output Power Level	MCS10	-	TBD	-	dBm
Target Output Power Level	MCS11	-	TBD	-	dBm
Transmit center frequency tolerance		-	-	TBD	ppm
Transmit Modulation Accuracy (EVM)	MCS10		-	-35	dB
	MCS11	-	-	-35	dB

2.4GHZ 802.11B RECEIVER

Item	Condition	Min.	Typ.	Max.	Unit
Receiver Minimum Input Level Sensitivity (PER< 8 %)	11Mbps	-	-88	-84	dBm
	1Mbps	-	-97	-93	dBm
Receiver Maximum Input Level Sensitivity (PER< 8 %)	11Mbps	-10	-	-	dBm
	1Mbps	-10	-	-	dBm

2.4GHZ 802.11G RECEIVER

Item	Condition	Min.	Typ.	Max.	Unit
Receiver Minimum Input Level Sensitivity (PER< 10%)	54Mbps	-	-75	-71	dBm
	6Mbps	-	-92	-88	dBm
Receiver Maximum Input Level (PER<10%)	54Mbps	-20	-	-	dBm
	6Mbps	-20	-	-	dBm

2.4GHZ 802.11N RECEIVER

Item	Condition	Min.	Typ.	Max.	Unit
SISO 2.4GHz – HT20 Receiver Input Level Sensitivity(PER<10%)	MCS7	-	-75	-71	dBm
	MCS0	-	-92	-88	dBm
SISO 2.4GHz – HT20 Receiver Maximum Input Level(PER<10%)	MCS7	-20	-	-	dBm
	MCS0	-20	-	-	dBm

2.4GHZ 802.11AC RECEIVER

Item	Condition	Min.	Typ.	Max.	Unit
SISO 2.4GHz – VHT20 Receiver Input Level Sensitivity(PER<10%)	MCS8	-	-72	-68	dBm
	MCS0	-	-92	-88	dBm
SISO 2.4GHz – VHT20 Receiver Maximum Input Level(PER<10%)	MCS8	-20	-	-	dBm
	MCS0	-20	-	-	dBm

2.4GHZ 802.11AX RECEIVER

Item	Condition	Min.	Typ.	Max.	Unit
SISO 2.4GHz – HE20	MCS11	-	-63	-59	dBm
Receiver Input Level Sensitivity(PER<10%)	MCS0	-	-92	-88	dBm
SISO 2.4GHz – HE20	MCS11	-20	-	-	dBm
Receiver Maximum Input Level(PER<10%)	MCS0	-20	-	-	dBm

5GHZ 802.11A RECEIVER

Item	Condition	Min.	Typ.	Max.	Unit
SISO Receiver Input Level Sensitivity	54Mbps	-	-74	-70	dBm
(PER<10%)	6Mbps	-	-91	-87	dBm
Receiver Maximum Input Level	54Mbps	-20	-	-	dBm
(PER<10%)	6Mbps	-20	-	-	dBm

5GHZ 802.11N RECEIVER 20MHZ

Item	Condition	Min.	Typ.	Max.	Unit
SISO Receiver Input Level Sensitivity	MCS7	-	-73	-69	dBm
(PER<10%)	MCS0	-	-91	-87	dBm
Receiver Maximum Input Level	MCS7	-20	-	-	dBm
(PER<10%)	MCS0	-20	-	-	dBm

5GHZ 802.11N RECEIVER 40MHZ

Item	Condition	Min.	Typ.	Max.	Unit
SISO Receiver Input Level Sensitivity	MCS7	-	-70	-66	dBm
(PER<10%)	MCS0	-	-88	-84	dBm
Receiver Maximum Input Level	MCS7	-20	-	-	dBm
(PER<10%)	MCS0	-20	-	-	dBm

5GHZ 802.11AC RECEIVER 20MHZ

Item	Condition	Min.	Typ.	Max.	Unit
SISO Receiver Input Level Sensitivity	MCS8	-	-69	-65	dBm
(PER<10%)	MCS0	-	-91	-87	dBm
Receiver Maximum Input Level	MCS9	-20	-	-	dBm
(PER<10%)	MCS0	-20	-	-	dBm

5GHZ 802.11AC RECEIVER 40MHZ

Item	Condition	Min.	Typ.	Max.	Unit
SISO Receiver Input Level Sensitivity	MCS9	-	-64	-60	dBm
(PER<10%)	MCS0	-	-88	-84	dBm
Receiver Maximum Input Level	MCS9	-20	-	-	dBm
(PER<10%)	MCS0	-20	-	-	dBm

5GHZ 802.11AC RECEIVER 80MHZ

Item	Condition	Min.	Typ.	Max.	Unit
SISO Receiver Input Level Sensitivity	MCS9	-	-62	-58	dBm
(PER<10%)	MCS0	-	-86	-82	dBm
Receiver Maximum Input Level	MCS9	-20	-	-	dBm
(PER<10%)	MCS0	-20	-	-	dBm

5GHZ 802.11AX RECEIVER

Item	Condition	Min.	Typ.	Max.	Unit
SISO 5GHz – HE20	MCS11	-	-60	-56	dBm
Receiver Input Level Sensitivity(PER<10%)	MCS0	-	-91	-87	dBm
SISO 5GHz – HE20	MCS11	-20	-	-	dBm
Receiver Maximum Input Level(PER<10%)	MCS0	-20	-	-	dBm
SISO 5GHz – HE40	MCS11	-	-58	-54	dBm
Receiver Input Level Sensitivity(PER<10%)	MCS0	-	-89	-85	dBm
SISO 5GHz – HE40	MCS11	-20	-	-	dBm
Receiver Maximum Input Level(PER<10%)	MCS0	-20	-	-	dBm
SISO 5GHz – HE80	MCS11	-	-55	-51	dBm
Receiver Input Level Sensitivity(PER<10%)	MCS0	-	-86	-82	dBm
SISO 5GHz – HE80	MCS11	-20	-	-	dBm
Receiver Maximum Input Level(PER<10%)	MCS0	-20	-	-	dBm
SISO 6GHz – HE20	MCS11	-	TBD	-	dBm
Receiver Input Level Sensitivity(PER<10%)	MCS0	-	TBD	-	dBm
SISO6GHz – HE20	MCS11	-	TBD	-	dBm
Receiver Maximum Input Level(PER<10%)	MCS0	-	TBD	-	dBm
SISO 6GHz – HE40	MCS11	-	TBD	-	dBm
Receiver Input Level Sensitivity(PER<10%)	MCS0	-	TBD	-	dBm
SISO 6GHz – HE40	MCS11	-	TBD	-	dBm
Receiver Maximum Input Level(PER<10%)	MCS0	-	TBD	-	dBm
SISO 6GHz – HE80	MCS11	-	TBD	-	dBm
Receiver Input Level Sensitivity(PER<10%)	MCS0	-	TBD	-	dBm

SISO 6GHz – HE80	MCS11	-	TBD	-	dBm
Receiver Maximum Input Level(PER<10%)	MCS0	-	TBD	-	dBm

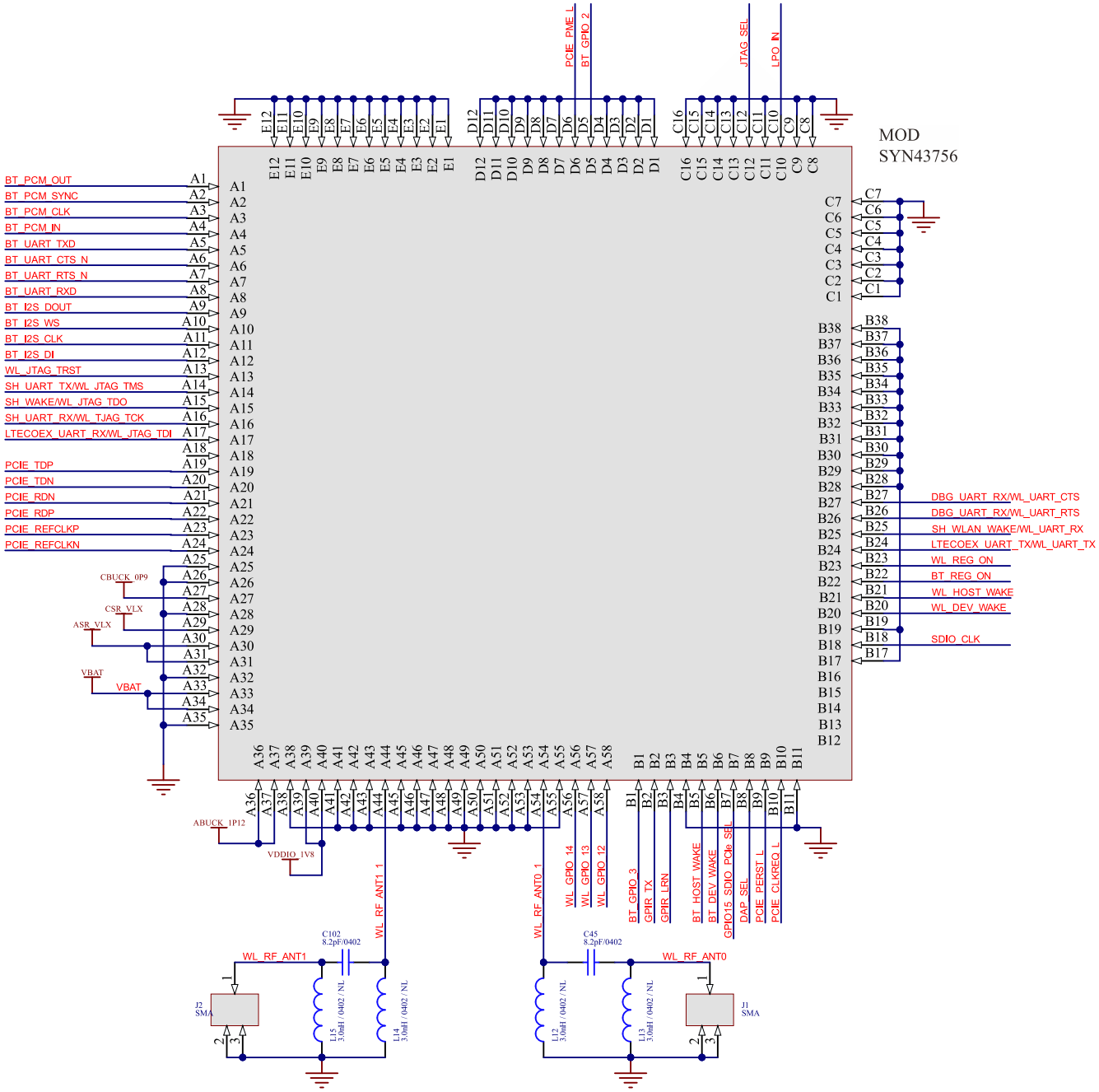
RADIO SPECIFICATIONS 802.15 BLUETOOTH

Features	Description
Frequency Band	2400 MHz ~ 2483.5 MHz
Number of Channels	79 channels
Modulation	FHSS (Frequency Hopping Spread Spectrum) , GFSK, DPSK

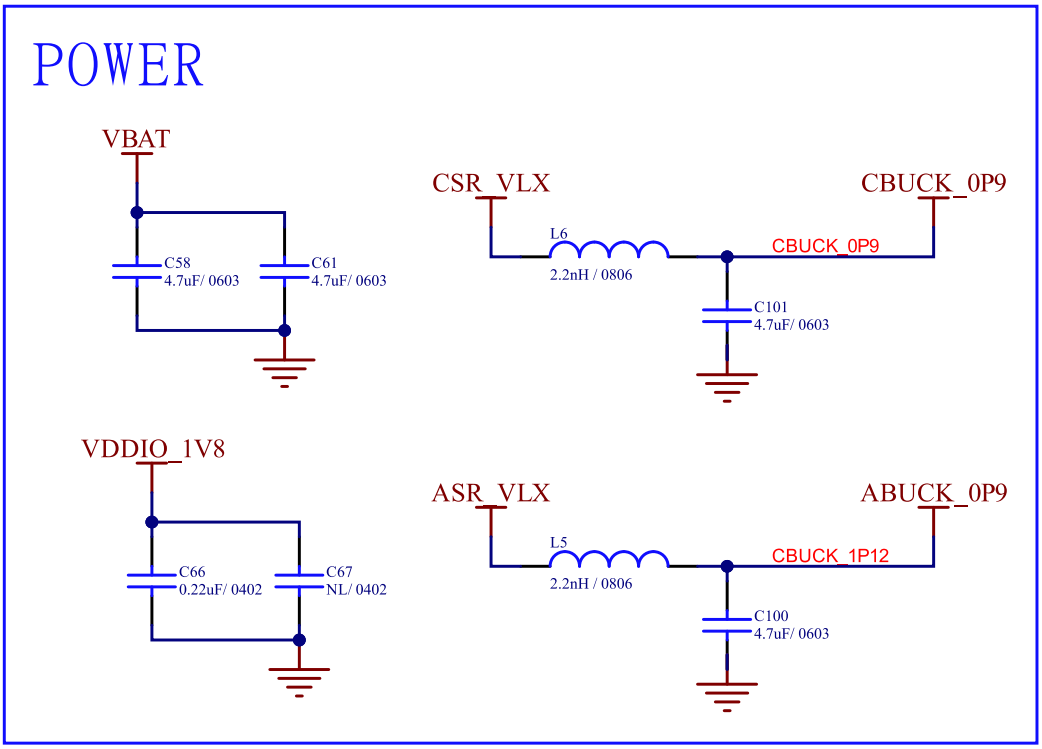
BLUETOOTH RADIO CHARACTERISTICS

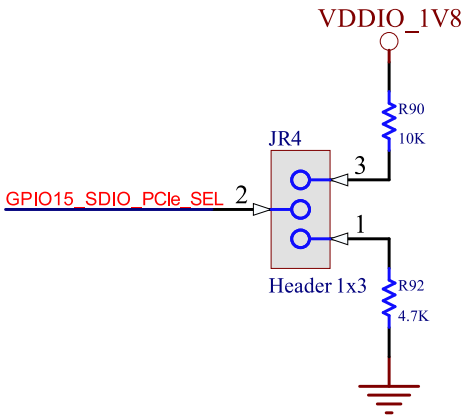
Parameter	Condition	Min.	Typ.	Max.	Unit
Basic Rate					
Output Power	Average Power	-	16	-	dBm
Frequency Range		2402	-	2480	MHz
Sensitivity (BER)	BER ≤ 0.1%	-	-91	-87	dBm
Maximum Input Level	BER ≤ 0.1%	-	0	-17	dBm
EDR					
Relative Power	π/4-DQPSK	-	10	-	dBm
	8DPSK	-	10	-	dBm
EDR Sensitivity(BER)	π/4-DQPSK BER ≤ 0.01%		-93	-89	dBm
	8DPSK BER ≤ 0.01%		-87	-83	dBm
EDR Maximum Input Level	π/4-DQPSK BER ≤ 0.01%	-	-	-17	dBm
	8DPSK BER ≤ 0.01%	-	-	-17	dBm
BLE					
BLE Output Power	BLE	-	16	-	dBm
	LE2	-	16	-	dBm
	LELR	-	16	-	dBm
BLE Sensitivity (PER)	125 kbps, LELR, 30.8% PER		-106.5	-102.5	dBm
	500 kbps, LELR, 30.8% PER		-101.5	-97.5	dBm
	2 Mbps, BLE, 30.8% PER		-94.5	-90.5	dBm
	2 Mbps, BLE, 30.8% PER		-91.5	-87.5	dBm
BLE Maximum Input Level	PER ≤ 30.8%	-	-	-17	dBm

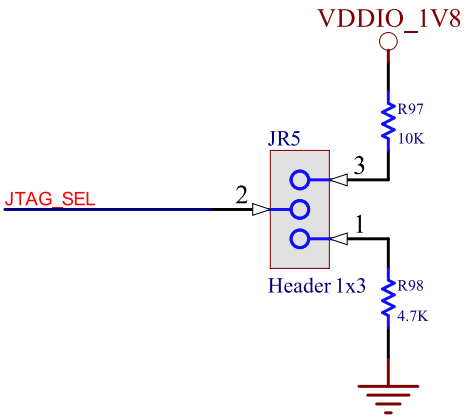
REFERENCE CIRCUIT

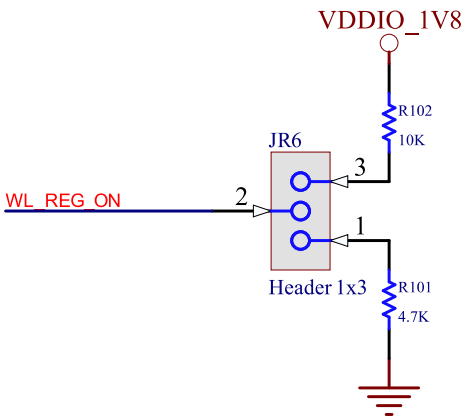


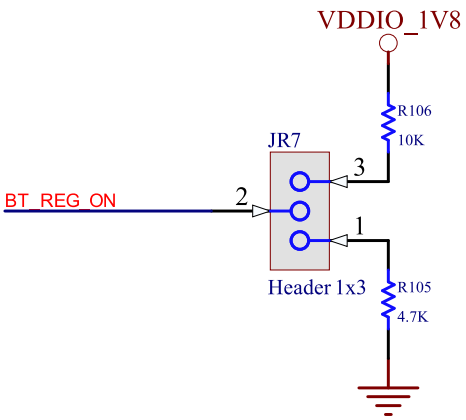
REFERENCE CIRCUIT







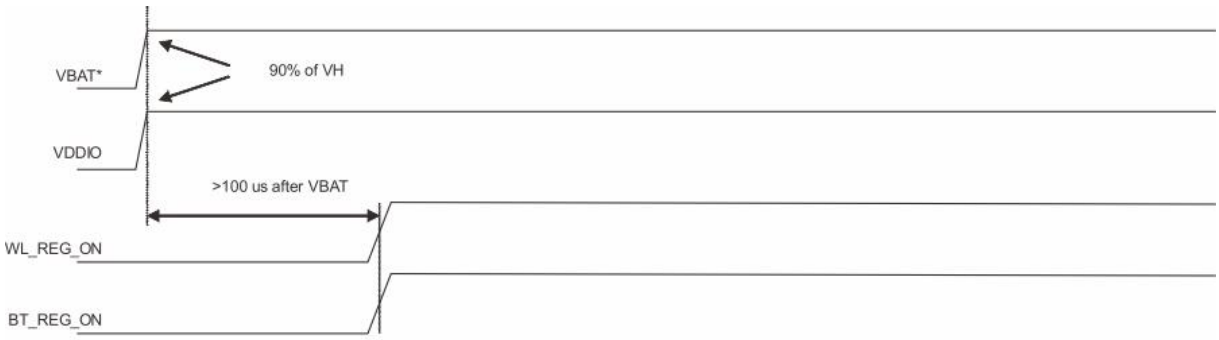




TIMING DIAGRAM OF INTERFACE

CONTROL SIGNAL TIMING DIAGRAMS

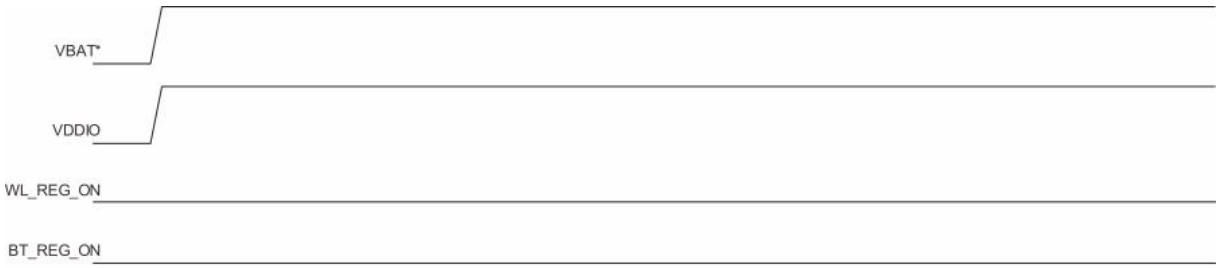
Power-up timing for WLAN ON, BT ON



***Notes:**
1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = ON, Bluetooth = ON

Power-up timing for WLAN OFF, BT OFF *



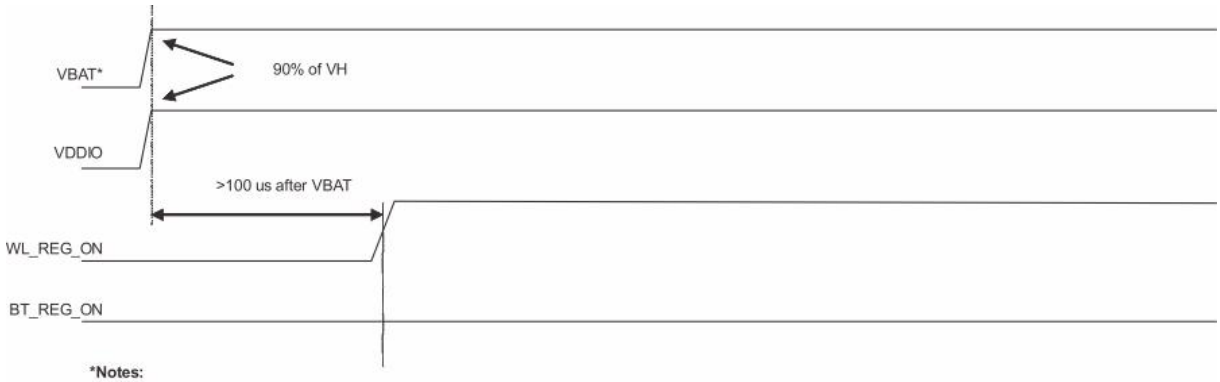
***Notes:**
1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = OFF

TIMING DIAGRAM OF INTERFACE

CONTROL SIGNAL TIMING DIAGRAMS

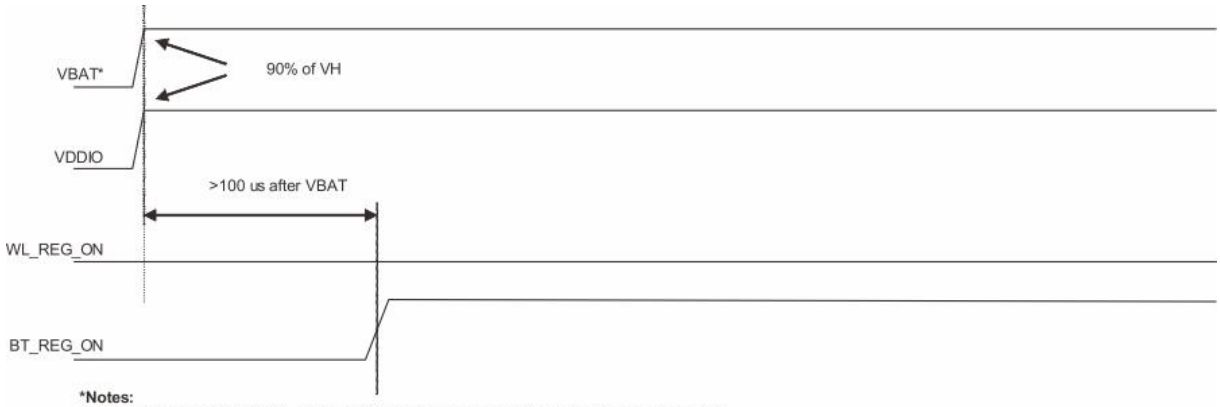
Power-up timing for WLAN ON, BT OFF *



***Notes:**
1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = ON, Bluetooth = OFF

Power-up timing for WLAN OFF, BT ON *



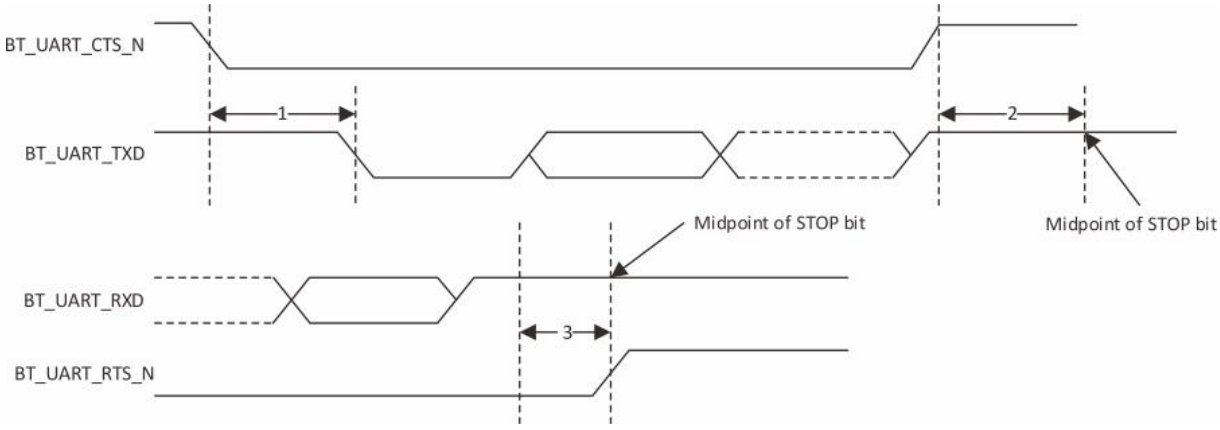
***Notes:**
1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN = OFF, Bluetooth = ON

TIMING DIAGRAM OF INTERFACE

UART TIMING

The SiP shares a single UART for Bluetooth. The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps.



Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_ UART_TXD valid	-	-	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	-	-	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_ RTS_N high	-	-	0.5	Bit periods

TIMING DIAGRAM OF INTERFACE

SDIO TIMING

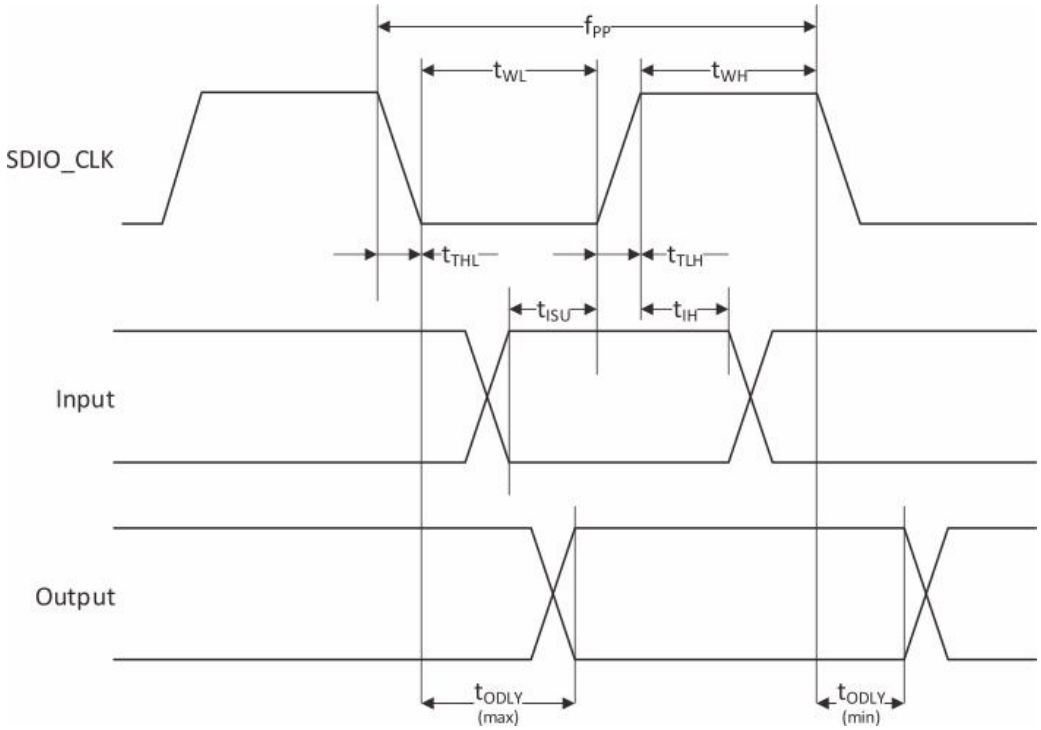
SiP WLAN section provides support for SDIO version 3.0 at 1.8V signaling, including the new UHS-I modes:

- DS: Default speed (DS) up to 25 MHz, including 1- and 4-bit modes.
- SDR12: SDR up to 25 MHz
- SDR25: SDR up to 50 MHz
- SDR50: SDR up to 100 MHz
- SDR104: SDR up to 208 MHz
- DDR50: DDR up to 50 MHz

Note:

- Per Section 6 of the SDIO specification, pull-ups in the 10 k to 100 k range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups
- The SYN43756 is backward compatible with SDIO v2.0 host interfaces.

SDIO timing in default mode



TIMING DIAGRAM OF INTERFACE

SDIO TIMING

SDIO Bus Timing Parameters (Default Mode)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[2])					
Frequency – Data Transfer mode	fPP	0	-	25	MHz
Frequency – Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time – Identification mode	tODLY	0	-	50	ns

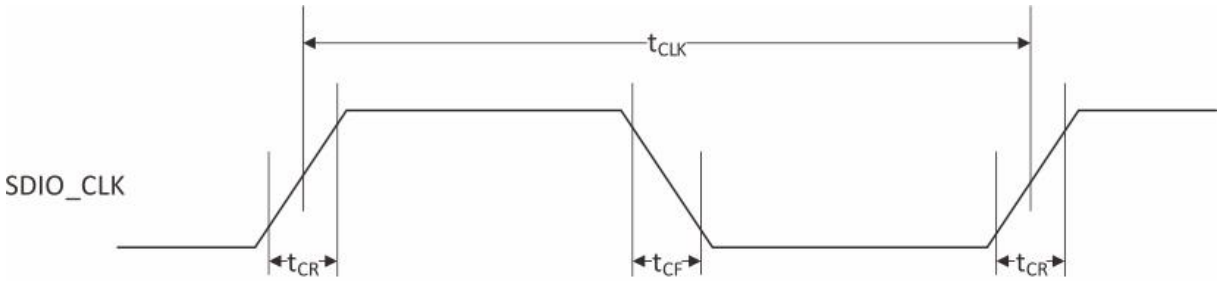
Note:

- Timing is based on CL ≤ 40 pF load on CMD and Data.
- Minimum (Vih) = 0.7 × VDDIO and maximum (Vil) = 0.2 × VDDIO.

TIMING DIAGRAM OF INTERFACE

SDIO Bus Timing Specifications in SDR Modes - Clock Timing

SDIO Clock Timing (SDR Modes)



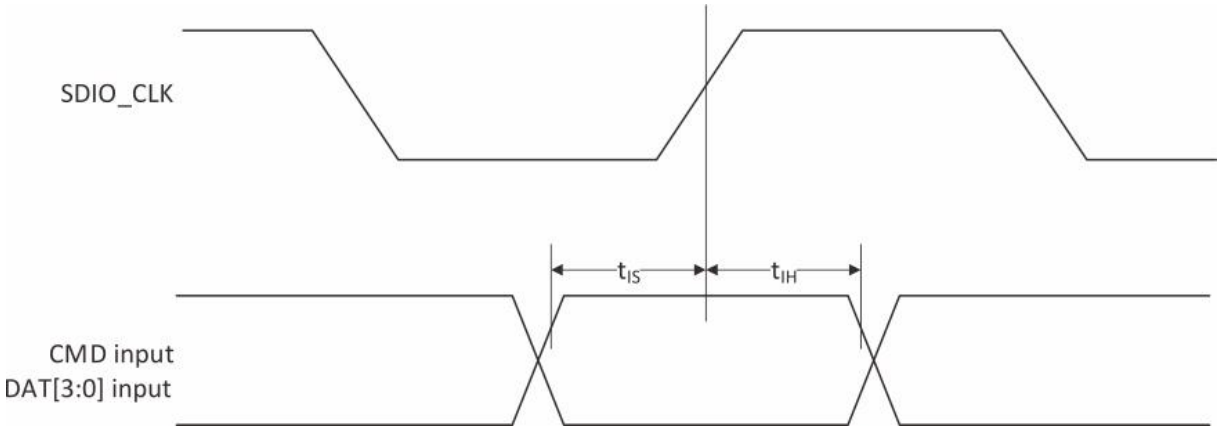
SDIO Bus Clock Timing Parameters (SDR Modes)

Parameter	Symbol	Min.	Max.	Unit	Comments
-	tCLK	40	-	ns	SDR12 mode
		20	-	ns	SDR25 mode
		10	-	ns	SDR50 mode
		4.8	-	ns	SDR104 mode
-	tCR, tCF	-	0.2 × tCLK	ns	tCR, tCF < 2.00 ns (maximum) @100 MHz, CCARD = 10 pF
Clock duty	–	30	70	%	–

TIMING DIAGRAM OF INTERFACE

Device Input Timing

SDIO Bus Input Timing (SDR Modes)



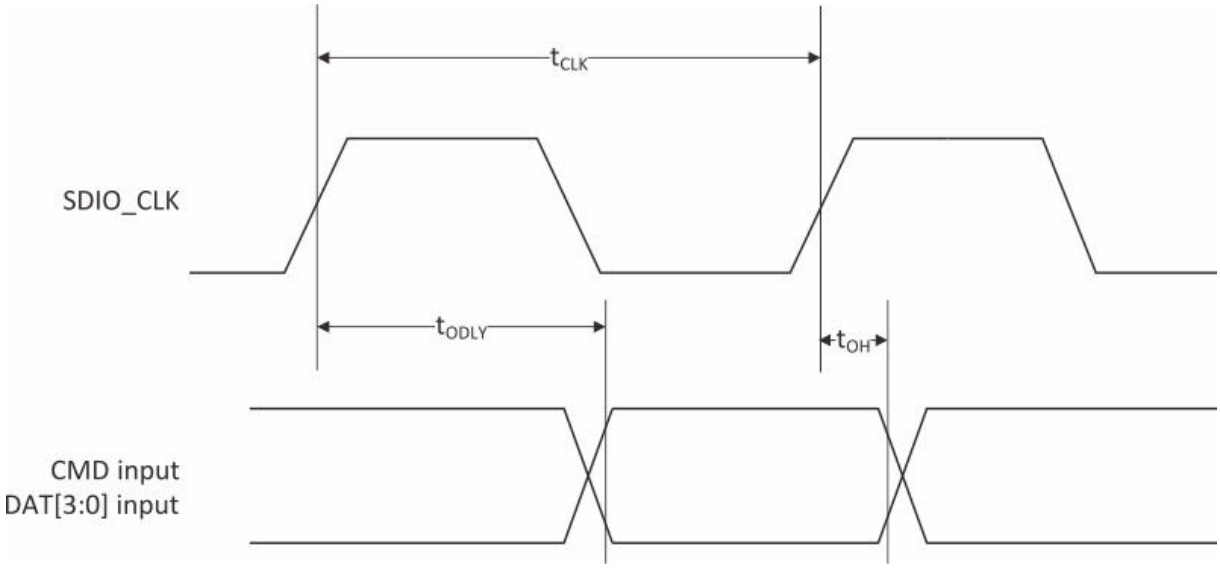
SDIO Bus Input Timing Parameters (SDR Modes)

Symbol	Min.	Max.	Unit	Comments
SDR104 Mode				
tIS	1.4	-	ns	CCARD = 10 pF, VCT = 0.975V
tIH	0.80	-	ns	CCARD = 5 pF, VCT = 0.975V
SDR50 Mode				
tIS	3.00	-	ns	CCARD = 10 pF, VCT = 0.975V
tIH	0.80	-	ns	CCARD = 5 pF, VCT = 0.975V

TIMING DIAGRAM OF INTERFACE

Device Output Timing

SDIO Bus Output Timing (SDR Modes up to 100 MHz)



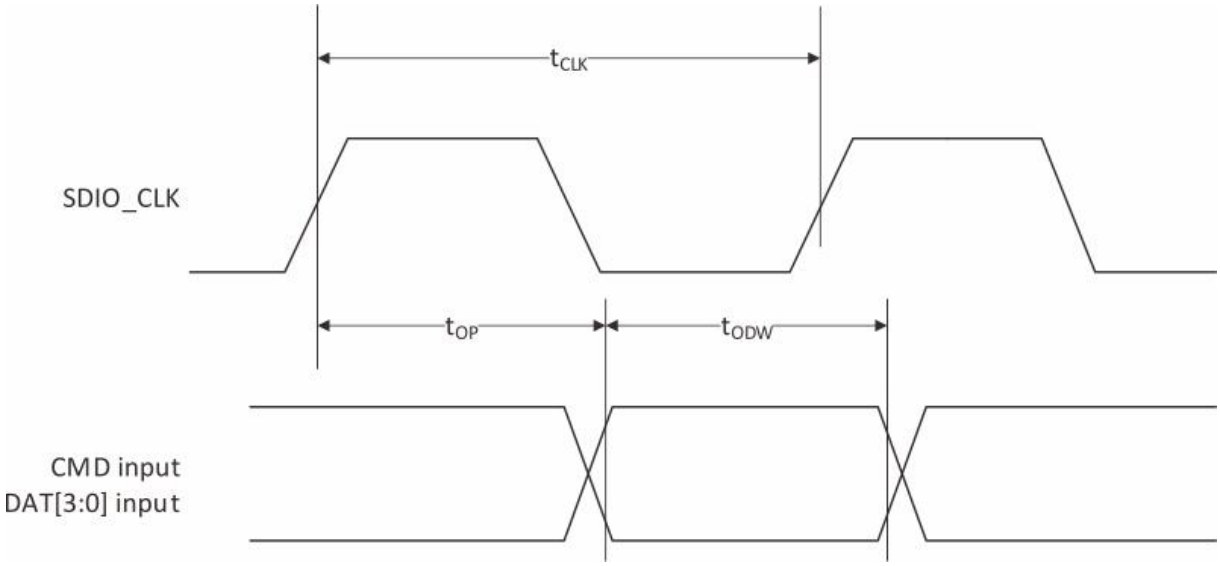
SDIO Bus Output Timing Parameters (SDR Modes up to 100 MHz)

Symbol	Min.	Max.	Unit	Comments
tODLY	-	7.5	ns	tCLK ≥ 10 ns CL= 30 pF using driver type B for SDR50
tODLY	-	14.0	ns	tCLK ≥ 20 ns CL= 40 pF using for SDR12, SDR25
tOH	1.5	-	ns	Hold time at the tODLY (min) CL= 15 pF

TIMING DIAGRAM OF INTERFACE

Device Output Timing

SDIO Bus Output Timing (SDR Modes 100 MHz to 208 MHz)



SDIO Bus Output Timing Parameters (SDR Modes 100 MHz to 208 MHz)

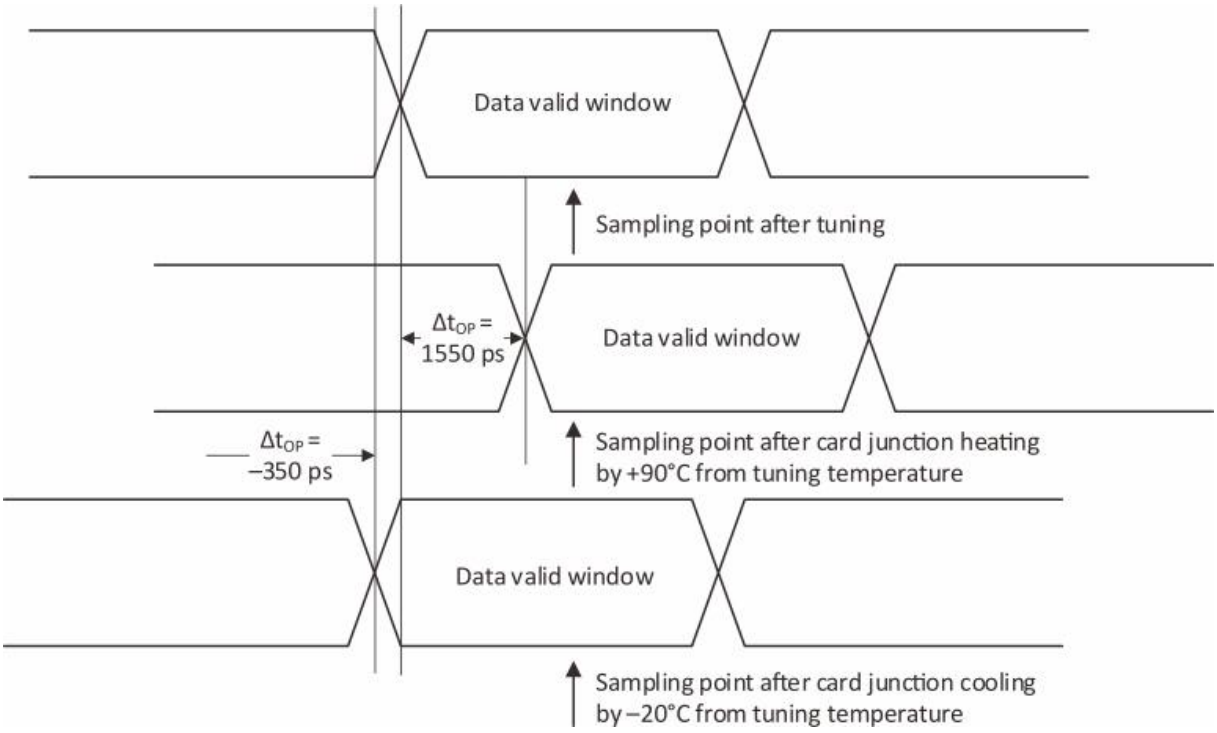
Symbol	Min.	Max.	Unit	Comments
tOP	0	2	UI	Card output phase
ΔtOP	-350	+1550	ps	Delay variation due to temperature change after tuning
tODW	0.60	-	UI	tODW = 2.88 ns @ 208 MHz

- Δ tOP = +1550 ps for junction temperature of ΔtOP = 90 degrees during operation
- Δ tOP = –350 ps for junction temperature of ΔtOP = –20 degrees during operation
- Δ tOP = +2600 ps for junction temperature of ΔtOP = –20 to +125 degrees during operatio

TIMING DIAGRAM OF INTERFACE

Device Output Timing

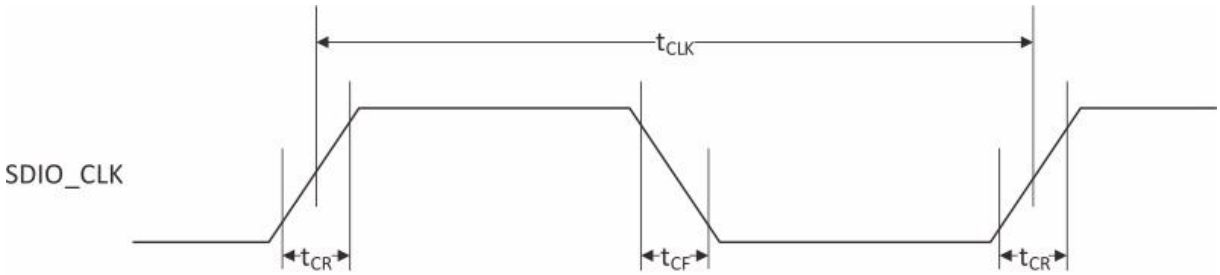
Δ tOP Consideration for Variable Data Window (SDR 104 Mode)



TIMING DIAGRAM OF INTERFACE

SDIO Bus Timing Specifications in DDR50 Mode

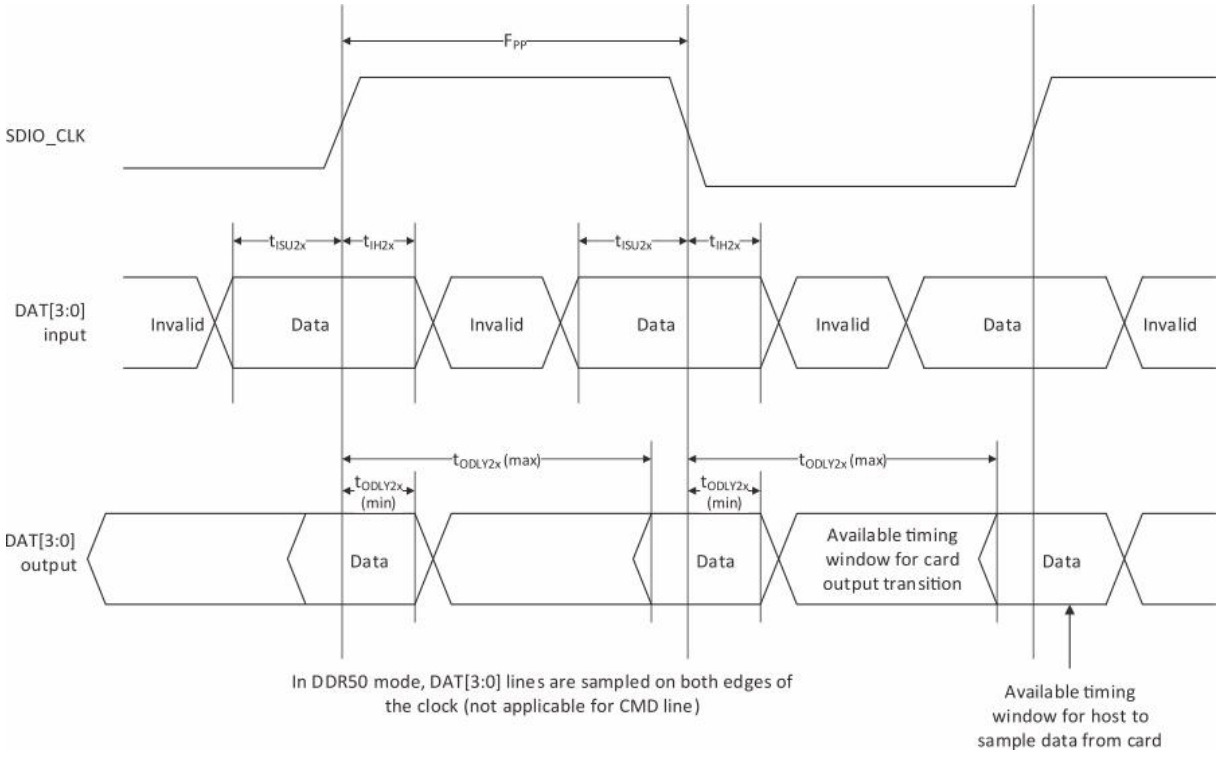
SDIO Clock Timing (DDR50 Mode)



SDIO Bus Clock Timing Parameters (DDR50 Mode)

Parameter	Symbol	Min.	Max.	Unit	Comments
-	tCLK	20	-	ns	DDR50 mode
-	tCR,tCF	-	0.2 × tCLK	ns	tCR, tCF < 4.00 ns (max) @ 50 MHz, CCARD = 10 pF
Clock duty	–	45	55	%	-

SDIO Data Timing (DDR50 Mode)



TIMING DIAGRAM OF INTERFACE

SDIO Bus Timing Specifications in DDR50 Mode

SDIO Bus Timing Parameters (DDR50 Mode)

Parameter	Symbol	Min.	Max.	Unit	Comments
Input CMD					
Input setup time	tISU	6	-	ns	CCARD < 10 pF (1 Card)
Input hold time	tIH	0.8	-	ns	CCARD < 10 pF (1 Card)
Output CMD					
Output delay time	tODLY	-	13.7	ns	CCARD < 30 pF (1 Card)
Output hold time	tOH	1.5	-	ns	CCARD < 15 pF (1 Card)
Input DAT					
Input setup time	tISU2x	3	-	ns	CCARD < 10 pF (1 Card)
Input hold time	tIH2x	0.8	-	ns	CCARD < 10 pF (1 Card)
Output DAT					
Output delay time	tODLY2x	–	7.5	ns	CCARD < 25 pF (1 Card)
Output hold time	tODLY2x	1.5	-	ns	CCARD < 15 pF (1 Card)

TIMING DIAGRAM OF INTERFACE

PCI EXPRESS TIMING

The PCI Express (PCIe) core on the Module is a high-performance serial I/O interconnect that is protocol compliant and electrically compatible with the PCI Express Base Specification v3.0 running at Gen2 speeds.

PCI Express Interface Parameters

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
General						
Baud rate	BPS	-	-	5	-	Gbaud
Reference clock peak-to- peak differential2	Vref	LVPECL, AC coupled	0.95	-	-	V
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40	50	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC- POS	Power-down or RESET high impedance	100k	-	-	Ω
Powered down termination (NEG)	ZRX-HIGH-IMP-DC- NEG	Power-down or RESET high impedance	1k	-	-	Ω
Input voltage	VRX-DIFFp-p	AC coupled, differential p-p	175	-	-	mV
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	-	-	UI
Differential return loss	RLRX-DIFF	Differential return loss	10	-	-	dB
Common-mode returnloss	RLRX-CM	Common-mode return loss	6	-	-	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET- DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition.	-	-	10	ms
Signal detect threshold	VRX-IDLE-DET- DIFFp-p	Electrical idle detect threshold	65	-	175	mV

TIMING DIAGRAM OF INTERFACE

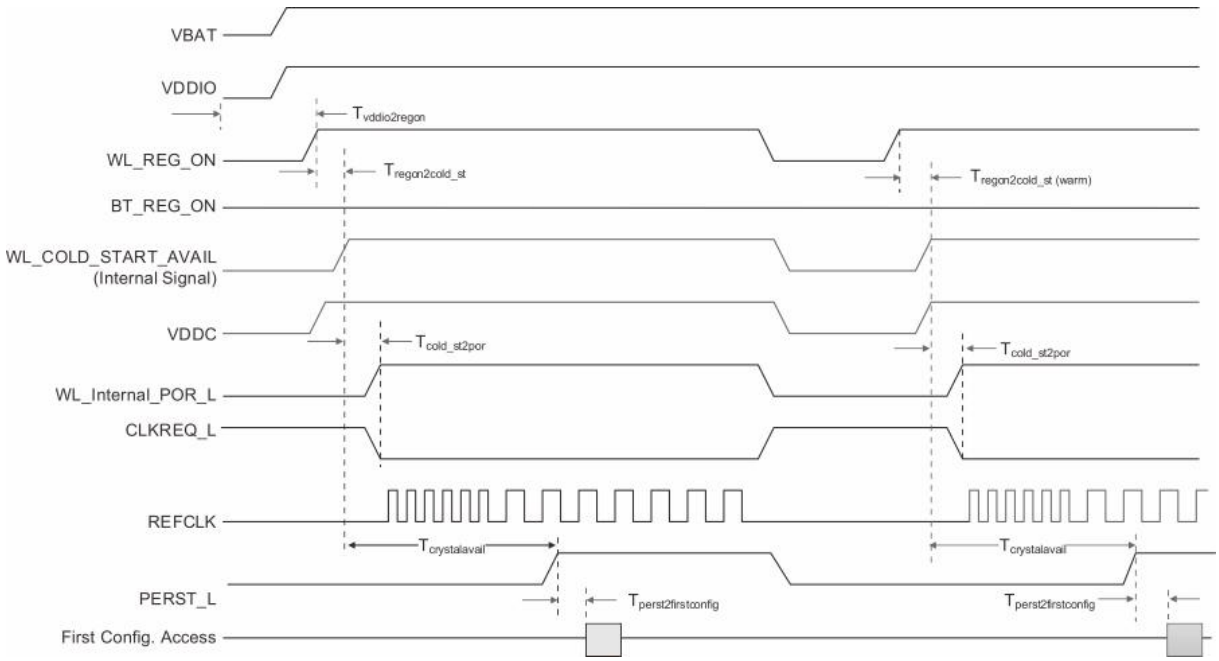
PCI EXPRESS TIMING

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Transmitter						
Output voltage	VTX-DIFFp-p	Differential p-p, programmable in 16 steps	0.8	-	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	-	-	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	-	-	UI
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection.	-	-	600	mV
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common-mode voltage (5 GT/s)	-	-	100	mV
TX AC peak common-mode voltage(2.5 GT/s)	VTX-CM-AC-P	TX AC common-mode voltage (2.5 GT/s)	-	-	20	mV
Absolute delta of DC common-mode voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-mode voltage during L0 and electricalidle.	0	-	100	mV
Absolute delta of DC common-mode voltage between D+ and D–	VTX-CM-DC-LINE- DELTA	DC offset between D+ and D–	0	-	25	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	-	20	mA
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground.	-	-	90	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80	-	120	Ω
Differential return loss	RLTX-DIFF	Differentialreturn loss	10 (min) for 0.05: 1.25 GHz	-	-	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6	-	-	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	-	-	UI

TIMING DIAGRAM OF INTERFACE

PCI EXPRESS TIMING

PCIe Power-On Timing Diagram



PCIe Power-On Timing Information

Timing Parameter	Notes	Value[a]	Unit
Tvddio2regon	-	0.1	ms
Tregon2cold_st	3.4 ms + 162 instruction-level parallelism (ILP) cycles	10.13	ms
Tcold_st2por	54 ILP cycles	2.24	ms
Tcrystalavail	509 ILP cycles	21.17	ms
Tperst2firstconfig	-	6.0	ms
Tvddioon2firstconfig	Tvddio2regon + Tregon2cold_st + Tcrystalavail + Tperst2firstconfig	37.4[b]	ms
Tregon2cold_st (warm)	162 ILP cycles	6.73	ms

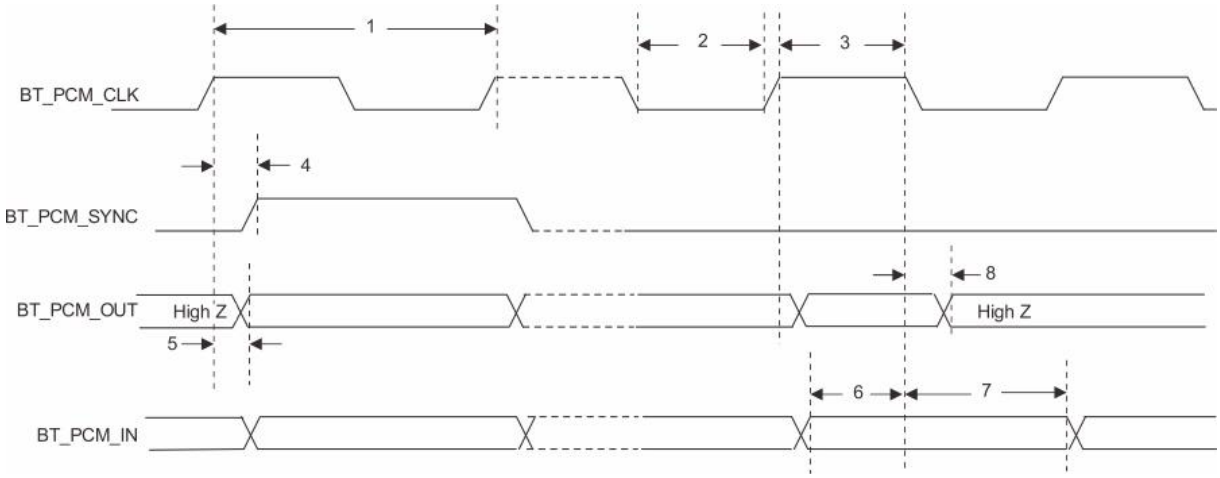
• (a) The time values assume an ILP tolerance of ±30%.
• (b) With VDDIO as a reference, 37.4 ms is the minimum system wait time before issuing the first configuration access.

TIMING DIAGRAM OF INTERFACE

PCM TIMING

The PCM Interface on the SiP can connect to linear PCM Codec devices in master or slave mode. In master mode, the SiP generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the SiP.

Short Frame Sync, Master Mode



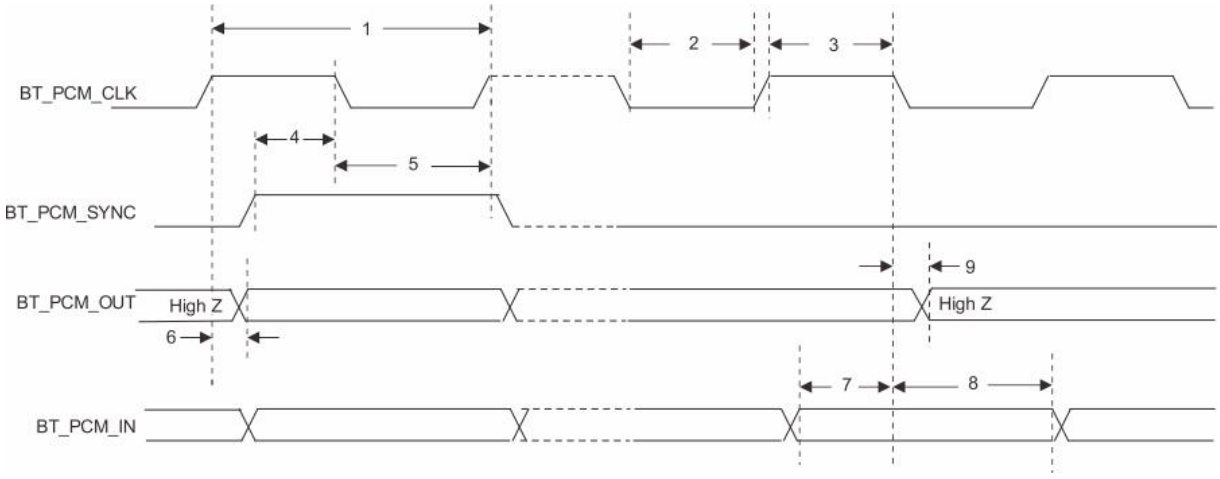
PCM Timing Diagram (Short Frame Sync, Master Mode)

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	BT_PCM_SYNC delay	0	-	25	ns
5	BT_PCM_OUT delay	0	-	25	ns
6	BT_PCM_IN setup	8	-	-	ns
7	BT_PCM_IN hold	8	-	-	ns
8	Delay from falling edge of BT_PCM_CLK during the last bit period to BT_PCM_OUT becoming high impedance.	0	-	25	ns

TIMING DIAGRAM OF INTERFACE

PCM TIMING

Short Frame Sync, Slave Mode

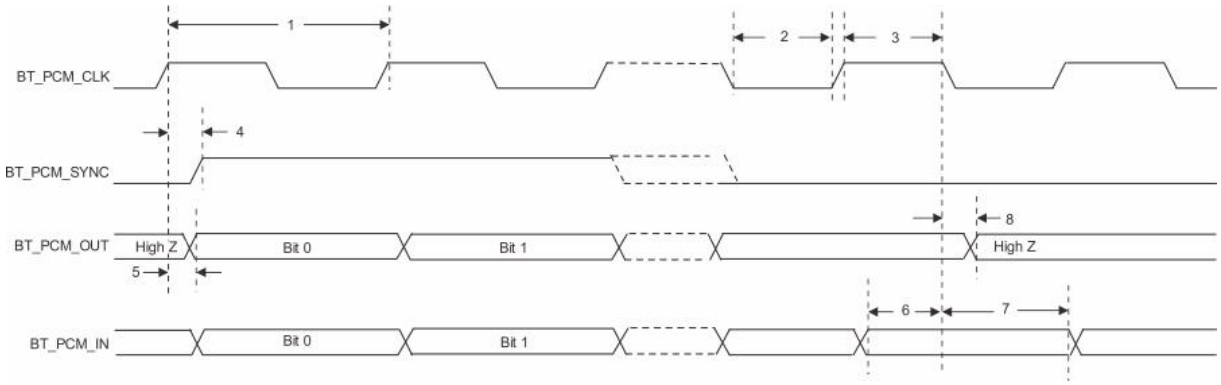


PCM Timing Diagram (Short Frame Sync, Slave Mode)

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	BT_PCM_SYNC setup	8	-	-	ns
5	BT_PCM_SYNC hold	8	-	-	ns
6	BT_PCM_OUT delay	0	-	25	ns
7	BT_PCM_IN setup	8	-	-	ns
8	BT_PCM_IN hold	8	-	-	ns
9	Delay from falling edge of BT_PCM_CLK during the last bit period to BT_PCM_OUT becoming high impedance.	0	-	25	ns

TIMING DIAGRAM OF INTERFACE

Long Frame Sync, Master Mode



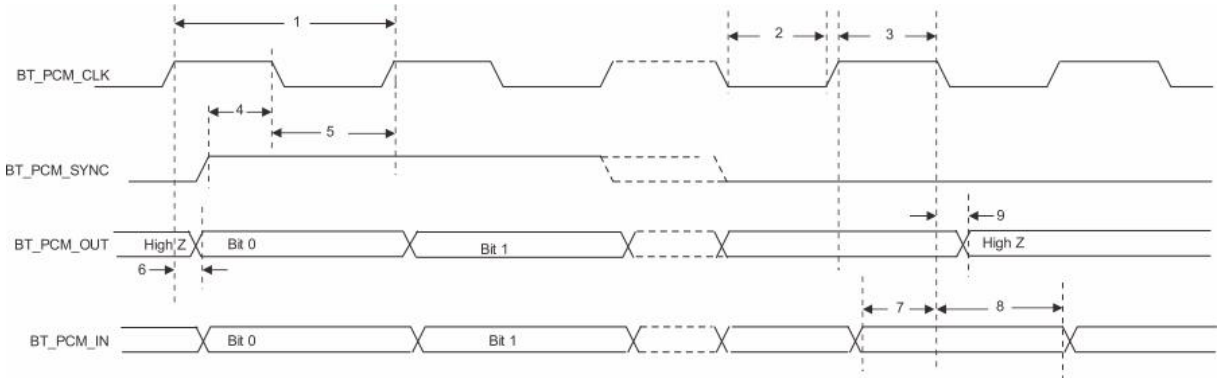
PCM Timing Diagram (Long Frame Sync, Master Mode)

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	BT_PCM_SYNC delay	0	-	25	ns
5	BT_PCM_OUT delay	0	-	25	ns
6	BT_PCM_IN setup	8	-	-	ns
7	BT_PCM_IN hold	8	-	-	ns
8	Delay from falling edge of BT_PCM_CLK during thelast bit period to BT_PCM_OUT becoming high impedance.	0	-	25	ns

TIMING DIAGRAM OF INTERFACE

PCM TIMING

Long Frame Sync, Slave Mode



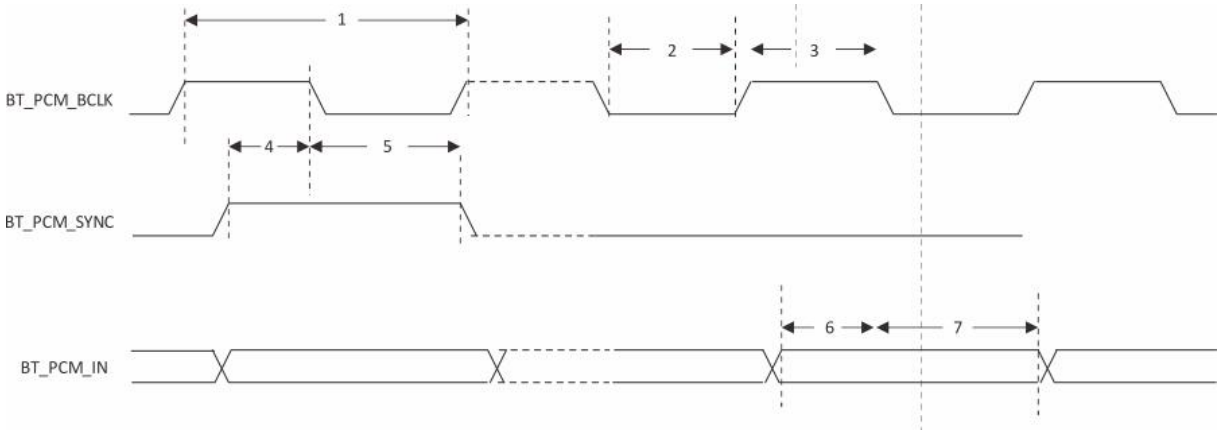
PCM Timing Diagram (Long Frame Sync, Slave Mode)

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	12	MHz
2	PCM bit clock low	41	-	-	ns
3	PCM bit clock high	41	-	-	ns
4	BT_PCM_SYNC setup	8	-	-	ns
5	BT_PCM_SYNC hold	8	-	-	ns
6	BT_PCM_OUT delay	0	-	25	ns
7	BT_PCM_IN setup	8	-	-	ns
8	BT_PCM_IN hold	8	-	-	ns
9	Delay from falling edge of BT_PCM_CLK during thelast bit period to BT_PCM_OUT becoming high impedance.	0	-	25	ns

TIMING DIAGRAM OF INTERFACE

PCM TIMING

Short Frame Sync, Burst Mode



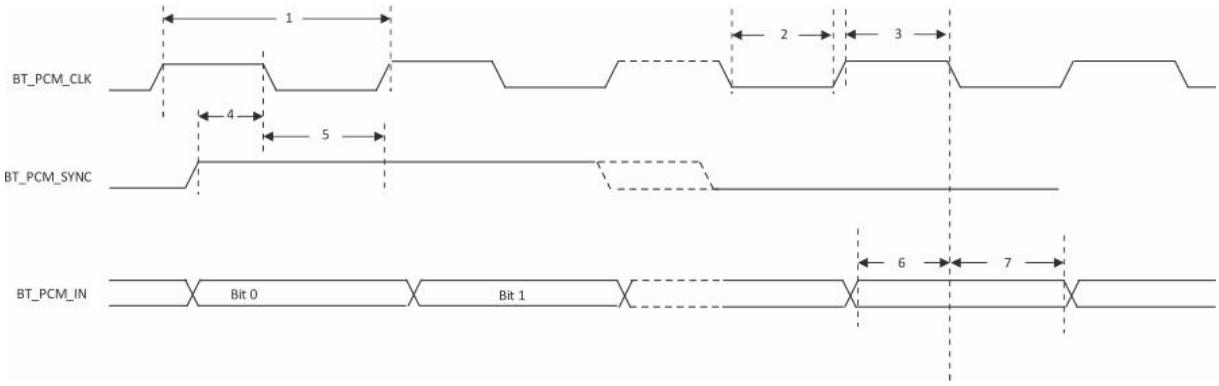
PCM Burst Mode Timing (Receive Only, Short Frame Sync)

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock low	20.8	-	-	ns
3	PCM bit clock high	20.8	-	-	ns
4	BT_PCM_SYNC setup	8	-	-	ns
5	BT_PCM_SYNC hold	8	-	-	ns
6	BT_PCM_IN setup	8	-	-	ns
7	BT_PCM_IN hold	8	-	-	ns

TIMING DIAGRAM OF INTERFACE

PCM TIMING

Long Frame Sync, Burst Mode



PCM Burst Mode Timing (Receive Only, Long Frame Sync)

Reference	Characteristics	Min.	Typ.	Max.	Unit
1	PCM bit clock frequency	-	-	24	MHz
2	PCM bit clock low	20.8	-	-	ns
3	PCM bit clock high	20.8	-	-	ns
4	BT_PCM_SYNC setup	8	-	-	ns
5	BT_PCM_SYNC hold	8	-	-	ns
6	BT_PCM_IN setup	8	-	-	ns
7	BT_PCM_IN hold	8	-	-	ns

TIMING DIAGRAM OF INTERFACE

I²S TIMING

The module supports an I²S digital audio port for Bluetooth audio. The I²S signals are:

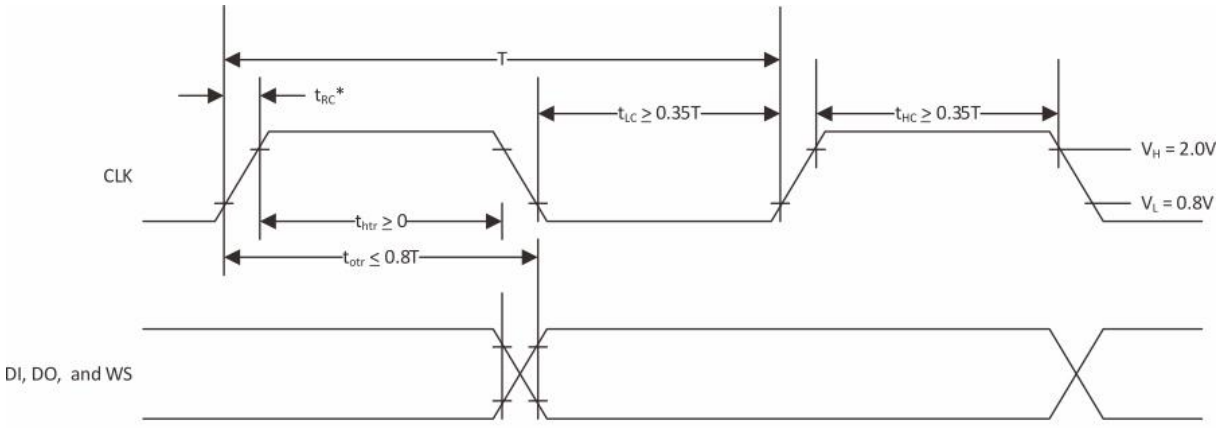
I²S clock: BT_ I²S_SCK

I²S Word Select: BT_ I²S_WS

I²S Data Out: BT_ I²S_DO

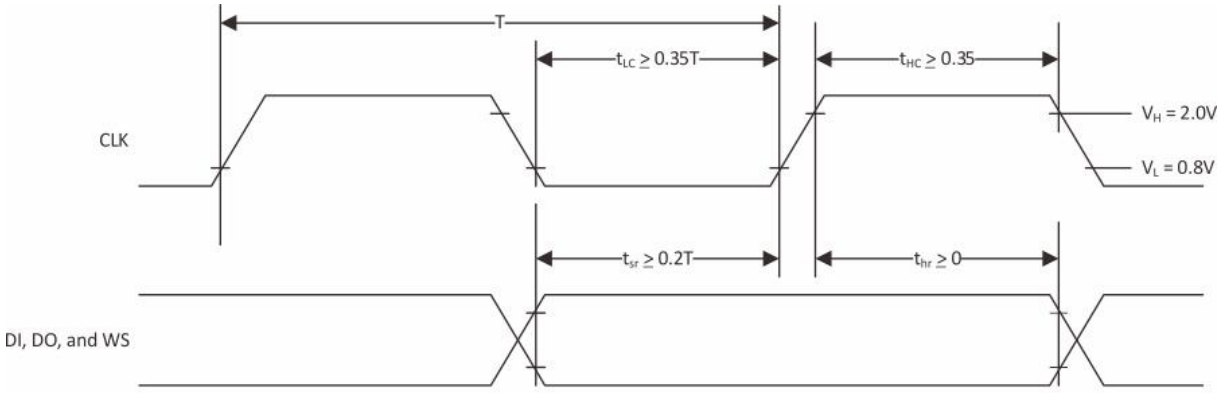
I²S Data In: BT_ I²S_DI

I²S Transmitter Timing



T = Clock period
T_{tr} = Minimum allowed clock period for transmitter
$T = T_{tr}$
* t_{RC} is only relevant for transmitters in slave mode.

I²S Receiver Timing



T = Clock period
T_r = Minimum allowed clock period for transmitter
$T > T_r$

TIMING DIAGRAM OF INTERFACE

I²S TIMING

	Transmitter				Receiver				Notes
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Clock period T	Ttr	-	-	-	Tr	-	-	-	1
Master Mode: Clock Generated by Transmitter or Receiver									
HIGH tHC	0.35Ttr	-	-	-	0.35Ttr	-	-	-	2
LOWtLC	0.35Ttr	-	-	-	0.35Ttr	-	-	-	2
Slave Mode: Clock Accepted by Transmitter or Receiver									
HIGH tHC	-	0.35Ttr	-	-	-	0.35Ttr	-	-	3
LOW tLC	-	0.35Ttr	-	-	-	0.35Ttr	-	-	3
Rise time tRC	-	-	0.15Ttr	-	-	-	-	-	4
Transmitter									
Delay tdtr	-	-	-	0.8T	-	-	-	-	5
Hold time thtr	0	-	-	-	-	-	-	-	4
Receiver									
Setup time tsr	-	-	-	-	-	0.2Tr	-	-	6
Hold time thr	-	-	-	-	-	0	-	-	6

- The system clock period T must be greater than Ttr and Tr because both the transmitter and receiver have to be able to handle the data transfer rate.
- At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, tHC and tLC are specified with respect to T.
- In slave mode, the transmitter and receiver need a clock signal with minimum high and low periods so that they can detect the signal. So long as the minimum periods are greater than 0.35Tr, any clock that meets the requirements can be used.
- Because the delay (tdtr) and the maximum transmitter speed (defined by Ttr) are related, a fast transmitter driven by a slow clock edge can result in tdtr not exceeding tRC which means thtr becomes zero or negative. Therefore, the transmitter has to guarantee that thtr is greater than or equal to zero, so long as the clock rise-time tRC is not more than tRCmax, where tRCmax is not less than 0.15Ttr.
- To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
- The data setup and hold time must not be less than the specified receiver setup and hold time.

4. SiP PIN ASSIGNMENT

Pin Name

Pin #	Pin Name	Type	Description
RF Port			
A54	ANT	I/O	WLAN/BT Transmit/Receive Antenna Port 0
A44	ANT	I/O	WLAN/BT Transmit/Receive Antenna Port 1
WLAN SDIO Interface			
B16	SDIO_DATA_0	I/O	SDIO Bus data line 0
B15	SDIO_DATA_1	I/O	SDIO Bus data line 1
B14	SDIO_DATA_2	I/O	SDIO Bus data line 2
B13	SDIO_DATA_3	I/O	SDIO Bus data line 3
B12	SDIO_CMD	I/O	SDIO Bus command line
B18	SDIO_CLK	I	SDIO Bus clock input
WLAN PCI Express Interface			
A21	PCIE_RDN0	I	Receiver differential pair (x1 lane)
A22	PCIE_RDP0	I	
A24	REFCLKN	I	PCIe differential clock input (x1 lane).
A23	REFCLKP	I	
A20	PCIE_TDN0	O	Transmitter differential pair (x1 lane)
A19	PCIE_TDP0	O	
D6	PCIE_PME_L	OD	PCI power management event output. Used to request a change in the device or system power state. The assertion and deassertion of this signal are asynchronous to the PCIe reference clock. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3.
B10	PCIE_CLKREQ_L	OD	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. 1 = the clock can be gated. 0 = the clock is required.
B9	PCIE_PERST_L	I	PCIe system reset. This input is the PCIe reset asdefined in the PCIe base specification version 1.1.

Pin Name

Pin #	Pin Name	Type	Description
Bluetooth UART Interface (level referred by VDDIO)			
A5	BT_UART_TXD	O	Bluetooth UART serial output. Serial data output for the HCI UART Interface.
A6	BT_UART_CTS_N	I	Bluetooth UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
A7	BT_UART_RTS_N	O	Bluetooth UART request-to-send. Active-low request-to-send signal for the HCI UART interface.
A8	BT_UART_RXD	I	Bluetooth UART serial input. Serial data input for the HCI UART Interface.
Bluetooth PCM Interface (level referred by VDDIO)			
A1	BT_PCM_OUT	O	PCM data output.
A2	BT_PCM_SYNC	I/O	PCM sync; can be master (output) or slave (input).
A3	BT_PCM_CLK	I/O	PCM clock; can be master (output) or slave (input).
A4	BT_PCM_IN	I	PCM data input.
Bluetooth I2S Interface (level referred by VDDIO)			
A9	BT_I2S_DO	I/O	I2S data output
A10	BT_I2S_WS	I/O	I2S WS; can be master (output) or slave (input)
A11	BT_I2S_CLK	I/O	I2S clock; can be master (output) or slave (input)
A12	BT_I2S_DI	I/O	I2S data input
Reference Clock			
C10	32kHz	I	External sleep clock input (32.768 kHz)
GPIO and Control Signal (level referred by VDDIO)			
B21	WL_HOST_WAKE	I	This pin can be programmed by software to be a GPIO or a WLAN_HOST_ WAKE output indicating that host wake-up should be performed.
B20	WL_DEV_WAKE	I	This pin can be programmed by software to be a GPIO or a WLAN_DEV_ WAKE output indicating that host wake-up should be performed.
B8	DAP_SEL	O	This pin can be programmed to be a GPIO, the DAP _SEL signal, UART_DBG_ TX or the GCI external coexistence interface. Debug access port select (DAP_SEL) 0: Not selected 1: Selected

Pin Name

Pin #	Pin Name	Type	Description
B24	LTECOEX_UART_ TX/WL_UART_TX	O	This pin can be programmed to be a GPIO, SPI_DATA_OUT signal, UART_TX or the GCI external coexistence interface.
B25	SH_WLAN_WAKE/ WL_UART_RX	OD	This pin can be programmed to be a GPIO, SPI_DATA_IN signal, UART_RX or the GCI external coexistence interface.
B26	DBG_UART_TX/ WL_UART_RTS	I/O	This pin can be programmed to be a GPIO, SPI_DATA_CLK signal, UART_RTS or the GCI external coexistence interface.
B27	DBG_UART_RX/ WL_UART_CTS	I/O	This pin can be programmed to be a GPIO, SPI_DATA_CS signal, UART_CTS or the GCI external coexistence interface.
A58	WL_GPIO_12	I/O	This pin can be programmed to be a GPIO, DBG_UART_RX or the GCI external coexistence interface.
A57	WL_GPIO_13	I/O	This pin can be programmed to be a GPIO, DBG_UART_TX or the GCI external coexistence interface.
A56	WL_GPIO_14	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
B7	GPIO15_SDIO_ PCIe_SEL	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
D5	BT_GPIO_2	I/O	Bluetooth general-purpose I/O
B1	BT_GPIO_3	I/O	Bluetooth general-purpose I/O
B2	GPIR_TX	I/O	Bluetooth general-purpose I/O or can be programmed to be Bluetooth IR transmit.
B3	GPIR_RX	I/O	Bluetooth general-purpose I/O or can be programmed to be Bluetooth IR learning.
B5	BT_HOST_WAKE	I/O	Bluetooth HOST_WAKE
B6	BT_DEV_WAKE	I/O	Bluetooth DEV_WAKE
B22	BT_REG_ON	I	Used by PMU to power up or power down the internal regulators used by the Bluetooth section. Also, when deasserted, this pin holds the Bluetooth section in reset. This pin has an internal 50 kΩ pull-down resistor that is autoenabled and disabled when the input is low and high, respectively.
B23	WL_REG_ON	I	Used by the PMU to power up or power down the internal regulators used by the WLAN section. When deasserted, this pin holds the WLAN section in reset. This pin has an internal 50 kΩ pull-down resistor that is auto-enabled and disabled when the input is low and high, respectively.

Pin Name

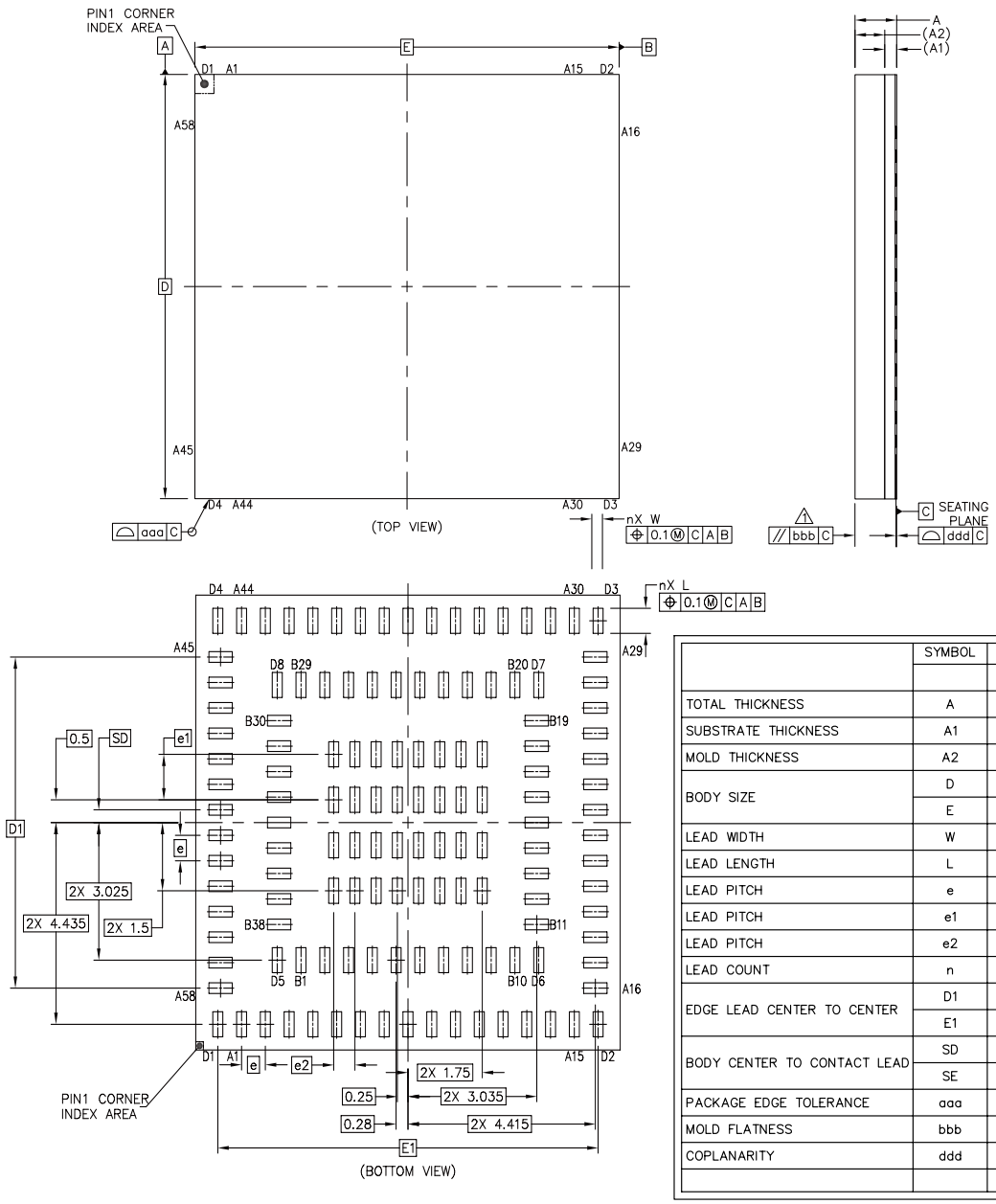
Pin #	Pin Name	Type	Description
JTAG Interface			
A13	WL_JTAG_TRST	I/O	This pin can be programmed to be a GPIO, the JTAG TRST signal, DBG_ UART_RX or the GCI external coexistence interface.
A14	SH_UART_TX/WL_ JTAG_TMS	I/O	This pin can be programmed to be a GPIO, the JTAG TMS signal, UART_TX or the GCI external coexistence interface.
A15	SH_WAKE/WL_ JTAG_TDO		This pin can be programmed to be a GPIO, the JTAG TDO signal, UART_RTS or the GCI external coexistence interface.
A16	SH_UART_RX/WL_ JTAG_TCK		This pin can be programmed to be a GPIO, the JTAG TCK signal, UART_RX or the GCI external coexistence interface.
A17	LTECOEX_UART_ RX/WL_JTAG_TDI		This pin can be programmed to be a GPIO, the JTAG TDI signal, UART_CTS or the GCI external coexistence interface.
C12	JTAG_SEL	I/O	JTAG select. This pin must be connected to ground if the JTAG interface is not used.
Power Supplies			
A33	VBAT	I	Battery supply for CBUCK power stage & Clean battery supplies for BTLDO3P3 and RFLDO3P3. Quiet supplies for CBUCK and ABUCK. PMU internal always-on domain.
A34			
A39	VDDIO	I	1.8V DC supply voltage input for digital I/O
A40			
A29	CSR_VLX	O	Core BUCK Regulator, connect external (2.2UH) inductor to CBUCK_0P9.
A27	CBUCK_0P9	I	Power supply for CBUCK_0P9 power rail & internal LDO, connect external (4.7UF) capacitor to ground.
A30	ASR_VLX	O	Analog BUCK Regulator, connect external (2.2UH) inductor to ABUCK_1P12.
A31			
A36	ABUCK_1P12	I	Power supply for ABUCK_1P12 power rail & internal LDO, connect external (4.7UF) capacitor to ground.
A37			

Pin Name

Pin #	Pin Name	Type	Description
Ground			
A18	GND		
A25-A26			
A28			
A32		-	Ground
A35		-	
A38		-	
A41-A43		-	
A45-A53		-	
A55		-	
B4		-	
B11		-	
B17		-	
B19		-	
B28-B38		-	
C1-C9		-	
C11		-	
C13-C14		-	
D1-D4		-	
D7-D12		-	
E1-E12		-	

5. PACKAGE OUTLINE

Outline Dimension

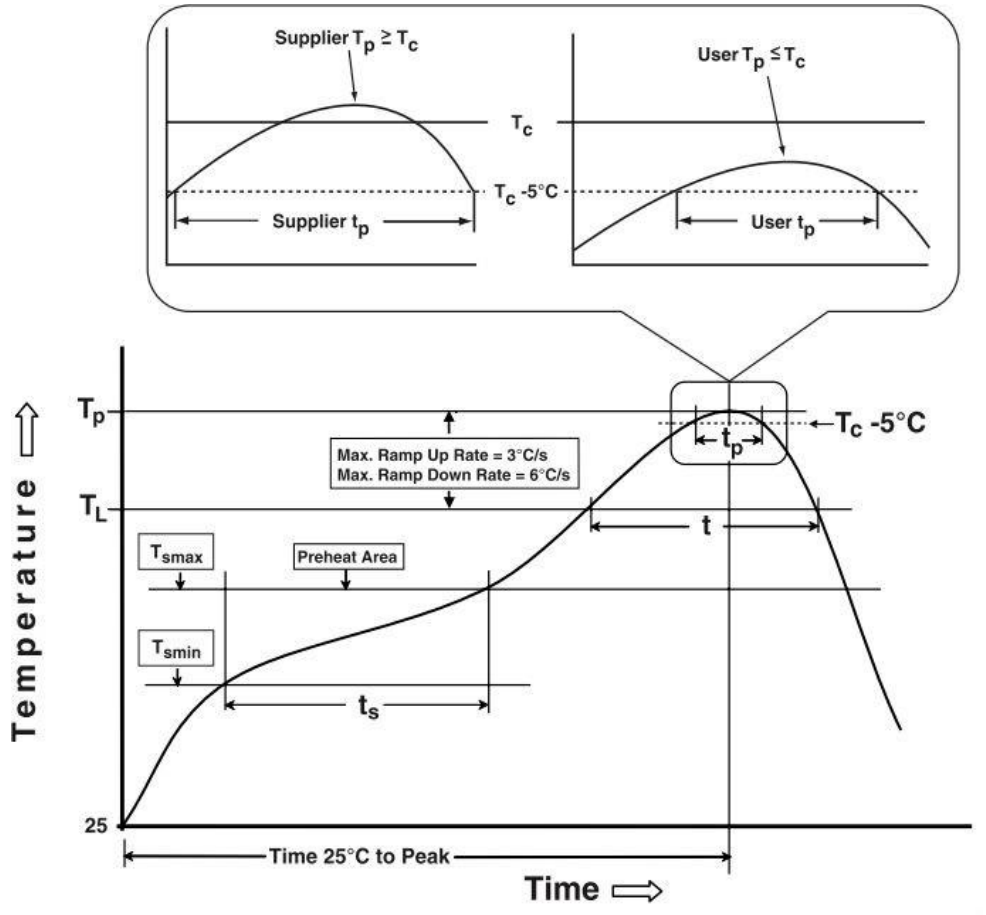


	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	0.932	0.982	1.1
SUBSTRATE THICKNESS	A1		0.282	REF
MOLD THICKNESS	A2		0.7	REF
BODY SIZE	D		10	BSC
	E		10	BSC
LEAD WIDTH	W	0.185	0.235	0.285
LEAD LENGTH	L	0.5	0.55	0.6
LEAD PITCH	e		0.56	BSC
LEAD PITCH	e1		1	BSC
LEAD PITCH	e2		0.5	BSC
LEAD COUNT	n		136	
EDGE LEAD CENTER TO CENTER	D1		7.28	BSC
	E1		8.96	BSC
BODY CENTER TO CONTACT LEAD	SD		0.28	BSC
	SE		---	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	

6. SPECIFICATION FOR REFLOW PROFILE

Reflow profiles

Critical Profiles Parameters	Pb-Free assembly
Preheat / Soak	
Temperature Min (Tsmin)	150° Celsius
Temperature Max (Tsmax)	200° Celsius
Time(ts) from (Tsmin to Tsmax)	60 ~ 120 seconds
Ramp-up rate (TL to Tp)	3° Celsius / second max
Liquidous temperature (TL)	217° Celsius
Time(tL) maintained above TL	60 ~ 150 seconds
Peak package body temperature (Tp)	260° Celsius ± 2° Celsius
Time(tp) within 5° C of the specified classification temperature (Tc), see Figure 5-1	30* seconds
Ramp-down rate (Tp to TL)	6° Celsius / second max
Time 25° C to peak temperature	8 minutes max



7. PACKAGE AND STORAGE CONDITION

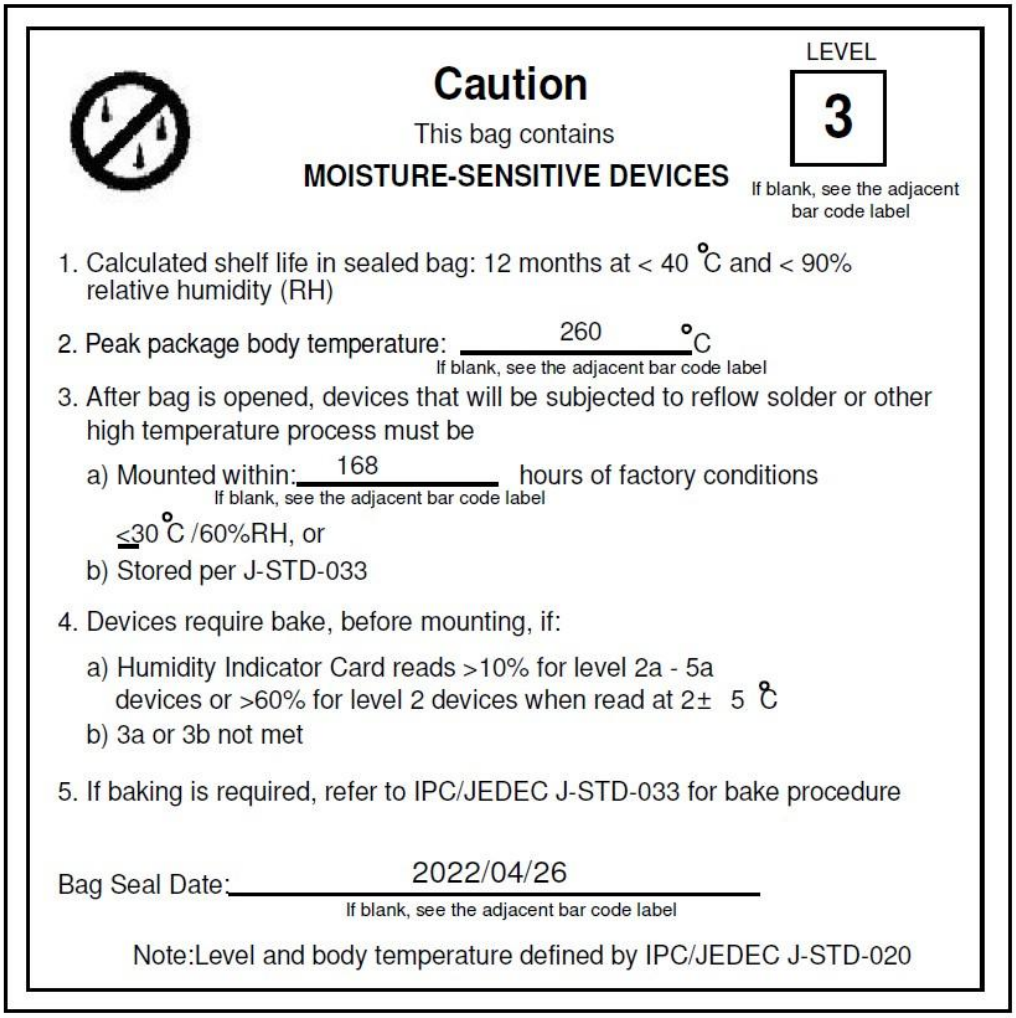
PACKAGE

TDB

EMC/ESD LEVEL

Surface Resistivity	Interior:10^{9}~10^{11}Ω/SQUARE
	EXTERIOR:10^{8}~10^{12}Ω/SQUARE
Dimension	475 x 420 mm
Tolerance	+5,0mm
Color	Background : Gray
	Text : Red

MSL LEVEL/STORAGE CONDITION



Caution

This bag contains

MOISTURE-SENSITIVE DEVICES

LEVEL **3**

If blank, see the adjacent bar code label

1. Calculated shelf life in sealed bag: 12 months at < 40 °C and < 90% relative humidity (RH)
2. Peak package body temperature: 260 °C
   If blank, see the adjacent bar code label
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
   a) Mounted within: 168 hours of factory conditions
   If blank, see the adjacent bar code label
   ≤30 °C /60%RH, or
   b) Stored per J-STD-033
4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card reads >10% for level 2a - 5a devices or >60% for level 2 devices when read at 2± 5 °C
   b) 3a or 3b not met
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: 2022/04/26
If blank, see the adjacent bar code label

Note:Level and body temperature defined by IPC/JEDEC J-STD-020

- Half-Sine Shock
- Sustained for Mechanical Shock under 2000G
- Life cycle: 1 year